A Survey of LC, Ring, and Active Inductor Oscillators

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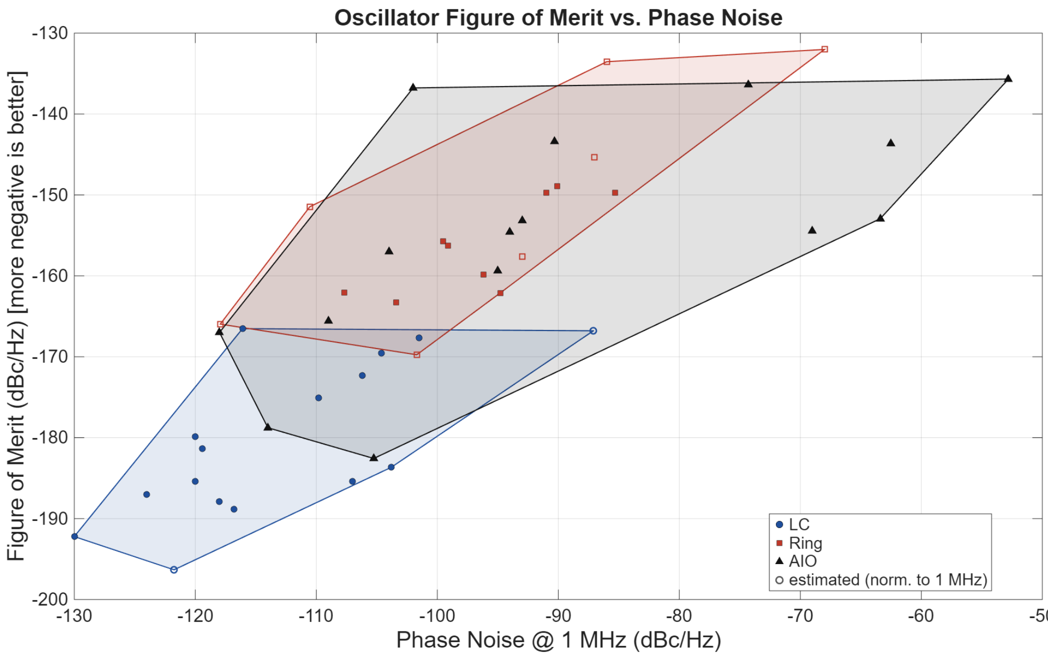

Figure 1: Oscillator design space: Figure of Merit vs. phase noise at 1 MHz offset for LC, ring and active inductor oscillators from the literature.

Abstract

The oscillator is an essential component in all communication systems. Crystal-free systems rely on free-running oscillators to eliminate the off-chip crystal. However, selecting the right type of oscillator requires a keen understanding of existing oscillator literature. This paper presents a survey of the major classes of integrated high frequency oscillators, particularly LC, ring and active inductor oscillators. A comparison on the basis of phase noise performance in the form of Figure of Merit (FoM) is presented along with the minimum achievable phase noise floors for different classes under a given power consumption. The goal is to help designers make better informed decisions when selecting an oscillator for a free-running crystal-free application. We found that the best ring oscillators in the literature are already at the edge of their minimum achievable phase noise, for a given power level, and hence, resonant oscillators such as LC and active inductor are the most promising path forward. Notably, active inductor designs remain comparatively underexplored despite their potential as an intermediate candidate between LC and ring oscillators; a gap this survey aims to motivate future work to address.

CCS Concepts

• **Hardware → Analog and mixed-signal circuits**; **Radio frequency and wireless circuits**; **Clock generation and timing**; *Wireline communication*; Energy generation and storage; On-chip resource management.

Keywords

RF oscillators, phase noise, jitter, Figure of Merit (FoM), design space exploration, literature review, Crystal-free IoT, Integrated Circuits

1 Introduction

Oscillators are essential for signal generation in modern communication and sensing systems. Traditional RF front-ends rely on crystal stabilized Phase-Locked Loops (PLLs) to meet the frequency accuracy requirements of standards such as IEEE 802.15.4 [1] and Bluetooth Low Energy (BLE) [2]. However, in the case of ultra-low-power IoT motes, with stringent size, cost, and integration constraints, the crystal reference becomes unfeasible [5, 40]. Without a crystal reference, the free-running on-chip oscillator must absorb the full burden of frequency stability including both temperature drift, and phase noise induced jitter [5, 32, 33]. Choosing the right type of oscillator requires a clear understanding of their phase noise performance, as well as power and area requirements.

Extensive research has been conducted on oscillator/VCO topologies to push the limits of frequency, phase noise, tunability and power consumption both in the context of crystal-free systems and traditional PLL based systems. The major CMOS oscillator families studied in the literature include LC oscillators (LCOs), Active Inductor Oscillators (AIOs), Ring Oscillators (ROs) and RC relaxation oscillators (RCOs). Crystal-free systems that use free-running on-chip LC tanks have successfully been used to demonstrate communications on IEEE 802.15.4 [1, 26] and Bluetooth Low Energy (BLE) [2, 45] standards. Further ongoing research aims to reduce the power and area of the RF front-end by removing the on-chip inductor in favor of ring or active inductor oscillators [33]. However, it is well known that each of these classes of oscillators has its own tradeoffs: RC/Ring oscillators are the smallest and run with the least power for a given frequency but tend to have the worst phase noise, whereas LC oscillators consume more power and area but provide better phase noise owing to their resonant quality factor Q [29]. Active inductor oscillators, composed of specially biased transistors to serve the function of an inductor in an oscillator transfer function, are comparatively under investigated outside of a few texts [41, 44, 46]. From the results of this work, we expect them to provide a middle ground between the two.

The theoretical foundation for this comparison is well established. Leeson's model provided the first closed form intuition for oscillator phase noise [21], while the impulse sensitivity function (ISF) framework of Hajimiri and Lee extended this to a rigorous, time varying treatment applicable to both LC and ring topologies [9, 10]. These frequency domain results connect to time domain stability metrics such as jitter and Allan deviation through well defined spectral integration relationships [3, 32, 49], and the combined body of work has driven substantial progress in low-power oscillator design for crystal-free radios [6, 18]. Navid *et al.* [29] reported the theoretical minimum achievable phase noise for RC relaxation and ring oscillators for a given power level under the ideal conditions of no colored noise and no dependence between the period jitters of independent cycles, i.e., only in the presence of thermal noise, while also noting that the phase noise of an LC oscillator is better than that of a relaxation/ring oscillator by a factor of Q^2 [29]. However, in a practical design, in the presence of flicker ($1/f$) and other colored noise sources, which is always the case for CMOS oscillators, these assumptions break down and the oscillator performs worse than this ideal limit, by what they named as the 'wastefulness factor'.

To get a more practical grasp of where the state-of-the-art is, a comparative survey of existing literature is needed. The few available surveys [36, 37] typically focus on a limited set of oscillator classes: [37] focuses primarily on LC oscillators only, and [36] focuses only on LC and ring oscillators. Active inductor oscillators are consistently under represented across the literature. Direct comparison across LC, active inductor and ring, particularly under unified normalization assumptions that account for frequency, power, and measurement offset, remains under reported. This gap is acutely limiting for crystal-free IoT design, where the designer must simultaneously consider power budgets in the sub-mW range, integration feasibility, and compliance with communication protocol timing margins.

This paper compares the current state-of-the-art of these major classes of on-chip oscillators, along with their ideal theoretical lower limits. We aim to answer a central question: what are the fundamental design trade-offs we can expect between phase noise, jitter, area, and power for a given oscillator class? To that end, we compiled a survey of published results for the major CMOS oscillator classes and placed them on common normalized axes so their measured performance can be compared directly. The main contribution of this paper includes a normalized dataset of published LC, active inductor and ring oscillator results drawn from the prior literature presented with a consistent normalization of heterogeneous reported metrics onto comparable phase noise, power, and Figure of Merit (FoM) axes [21] [19]. A comparative view of where each oscillator class sits in this space, including its practical performance bracket relative to the theoretical limits is also presented. Notably, comparatively little research has addressed active inductor designs despite their potential as an intermediate candidate. Our hope is that this survey motivates further investigation of this underexplored class.

2 Methodology

The dataset collects 50 published CMOS oscillator designs reported from 2004 to 2025, spanning the architectural families: LC, ring, and active inductor. The dataset composition is summarized in Table 1. Designs are reported with varying frequencies, phase noise offsets, power supplies, and FoM conventions, so they need to be normalized for fair comparison. This section sets up the basis for comparison: the theoretical minimums that bound oscillator phase noise for a given power consumption, and the figure of merit and offset conventions used to place designs on common axes.

2.1 Phase Noise Offset Normalization

Reported phase noise offsets span 100 kHz to 10 MHz (most commonly 1 MHz, but also 600 kHz, 3 MHz, and 10 MHz). To normalize these to a single offset, all values are translated to a common 1 MHz offset assuming a −20 dB/decade slope region.

$$L(1\ \text{MHz}) = L(\Delta f) - 20\log_{10}\left(\frac{1\ \text{MHz}}{\Delta f}\right). \tag{1}$$

2.2 Figure of Merit

To compare designs that operate at different frequencies and power levels, phase noise, frequency, and power are combined into the standard oscillator figure of merit:

$$\text{FoM} = L(\Delta f) - 20\log_{10}\left(\frac{f_{osc}}{\Delta f}\right) + 10\log_{10}\left(\frac{P}{1\ \text{mW}}\right), \tag{2}$$

which is the common benchmarking metric for CMOS oscillators. Note that this formulation results in negative FoM numbers as in [24], though a positive convention is also sometimes reported as in [22]. If the authors found a positive convention, it has been made negative for the purposes of this paper.

2.3 Minimum Phase Noise Floor

Phase noise in every one of these architectures arises from the up-conversion of device and thermal noise through a nonlinear, time varying mechanism, according to the impulse sensitivity based formulations of Hajimiri and Lee [9, 10]. Under the ideal assumptions that there are no colored noise sources in the circuit and there is no interdependence between period jitters, or in other words; the transistors are ideal with zero flicker noise, and the only noise type present is white thermal noise, the minimum achievable phase noise for a relaxation oscillator running with a given power consumption can be computed using Navid's model [29] as:

$$PN_{relax,\min}(\Delta f) \approx \frac{5.9\, f_o kT}{Cv_{dd}^2(\Delta f)^2} \approx \frac{3.1\, kT}{P_{\min}}\left(\frac{f_o}{\Delta f}\right)^2 \quad (3)$$

Similarly, for a ring oscillator [29]:

$$PN_{ring,\min}(\Delta f) \approx \frac{7.33\, f_o kT}{NCv_{dd}^2(\Delta f)^2} = \frac{7.33\, kT}{P_{\min}}\left(\frac{f_o}{\Delta f}\right)^2 \quad (4)$$

LC oscillators reach high Q_{eff} through resonant energy storage, and their phase noise is $\frac{1}{Q^2}$ better than ring/relaxation oscillators [29]. These formulations are used to compute the best case theoretical minimum noise floor that can be used for each class of oscillators. Although the quality factors of LC oscillators vary, based on our spiral design experience at 2.4 GHz we assume the ceiling for inductor quality factor is 30. As such, a pseudo minimum phase noise floor of 30 dB less than that of ring/relaxation oscillators is used for LC oscillators. Comparing the floor with the measured results, the wastefulness factor is computed as:

$$\Delta PN = PN_{meas} - PN_{min} \quad (5)$$

2.4 Minimum FoM Floor

The minimum phase noise floor of [29] still depends on the switching power P_{min} which makes it difficult to compare oscillators operating at different power levels. Hence it is better to compare oscillators through their minimum FoM, which can be computed as:

$$\mathrm{FoM}_{min} = PN_{min}(\Delta f) - 20\log_{10}\left(\frac{f_o}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{min}}{1\ \mathrm{mW}}\right). \quad (6)$$

Writing the minimum phase noise of Eqs. (4) and (3) compactly as $PN_{min} = 10\log_{10}\left[\alpha\, kT\, (f_o/\Delta f)^2/P_{min}\right]$, with $\alpha = 7.33$ for ring and $\alpha = 3.1$ for relaxation oscillators, and substituting into Eq. (6), both the carrier to offset ratio and the power cancel resulting in:

$$\begin{aligned}\mathrm{FoM}_{min} &= 10\log_{10}\left(\alpha\, kT\, \frac{(f_o/\Delta f)^2}{P_{min}}\right) \\ &\quad - 20\log_{10}\left(\frac{f_o}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{min}}{1\ \mathrm{mW}}\right) \\ &= 10\log_{10}(\alpha\, kT) + 30, \quad (7)\end{aligned}$$

The additive constant of 30 reflects the 1 mW reference of the figure of merit. The minimum FoM is therefore a single number, independent of both carrier frequency and power. This is the key advantage of working in the FoM domain. While the minimum phase noise of Eq. (4) traces a surface over the frequency/power plane, the minimum FoM collapses to one constant per oscillator class, appearing as a single horizontal line on a FoM versus frequency plot for a given temperature. At $T = 300$ K this evaluates to ≈ -165 dBc/Hz for ring and ≈ -169 dBc/Hz for relaxation oscillators. In the absence of resonance or other filtration techniques, every physically realizable design must lie above (i.e., have a less negative FoM than) its class floor, and the margin between a design's measured FoM and this floor is a power and frequency normalized measure of how far its colored (e.g., flicker) noise pushes it beyond the thermal noise limit.

The same construction extends to LC and active-inductor oscillators once their minimum phase noise is known. As noted in Section 2.3, an LC oscillator improves on the relaxation limit by a factor of Q^2 through the Leeson model, lowering its FoM floor by $20\log_{10} Q$; the active-inductor case is expected to behave similarly. Because the loaded quality factor Q is not consistently reported across the surveyed designs, these resonant floors are deferred to future work, and the present analysis adopts a fixed placeholder offset of 30 dB in their place.

3 Current State of the Art

This section presents the data collected and compares the three different classes of oscillators. The oscillator classes are plotted on three different planes: carrier frequency versus power to compare the maximum frequency per unit power (GHz/mW), measured phase noise versus expected thermal noise floor to compare colored noise suppression, and finally, FoM versus carrier frequency for a holistic comparison. Finally, the FoM trend over publication years is shown to depict the advancements in each oscillator class's state-of-the-art.

3.1 Power Vs Frequency

It can be observed in Fig. 2 that the LC and ring oscillators occupy distinct regions in the power consumption versus carrier frequency plot, with some overlap, while active inductor oscillators cover the whole design space. LC designs are able to generate similar frequencies for lower power than ring oscillators, reaching close to sub-mW power levels for GHz frequencies [7, 11–14, 16, 27, 30, 34, 35, 38, 39, 43, 47, 48]. Ring oscillator designs sit at much higher power levels [8, 15, 17, 24, 31]. Active inductor designs reach the

Table 1: Per-class composition and performance brackets (50 entries, 2004–2025).

Class	f_{osc} (GHz)	PN@1 MHz (dBc/Hz)		FoM (dBc/Hz)		Power (mW)
	range	best	worst	best	worst	range
LC (18)	1.0–90	−130.3	−87.1	−196.3	−166.5	0.048–87
Ring (17)	0.49–8.1	−117.9	−68.0	−169.8	−132.0	0.045–100
Active inductor (15)	0.29–12.7	−118.0	−52.8	−182.6	−135.7	0.031–54

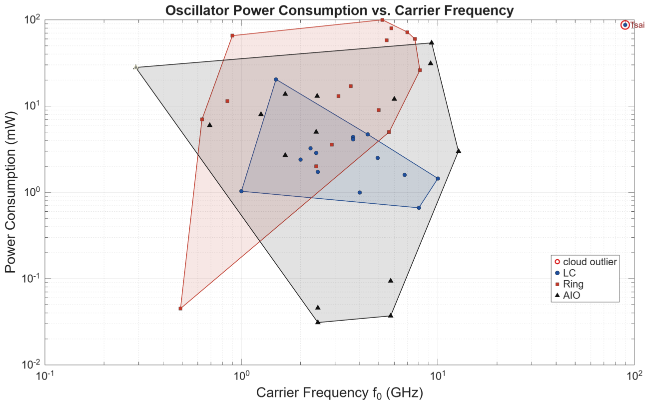

Figure 2: Carrier frequency versus power consumption for the surveyed oscillators with per class clouds. Outliers are ringed and labeled.

lowest power for some of the higher frequencies [4, 20, 23, 25, 28, 42, 46, 50].

3.2 Noise Floors and Figure of Merit

The three-dimensional view of Fig. 3 gives a visual depiction of the three main components in an oscillator FoM, i.e., power consumption, carrier frequency, and phase noise. The minimum phase noise floors of Eqs. (4) and (3) [29] become surfaces in this plot. The surface resulting from Eq. (4) is shown, and a pseudo reference for LC/active inductor topologies is drawn 30 dB below that.

Presenting the data of Fig. 3 using a FoM, instead of phase noise, we get the FoM versus carrier frequency plane shown in (Fig. 4), and for a temperature of $300K$, the minimum phase noise floor planes become lines at -165 dBc/Hz for ring, and ≈ -195 dBc/Hz for the resonant classes.

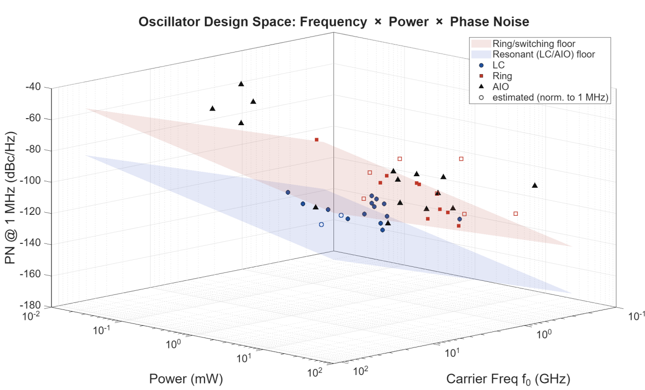

Figure 3: Three dimensional view of the design space: carrier frequency, power, and phase noise at 1 MHz offset. The red translucent surface is the thermal noise floor at $T = 300K$ for ring oscillators, and blue surface is a pseudo floor for LC oscillators placed 30 dB below the ring floor.

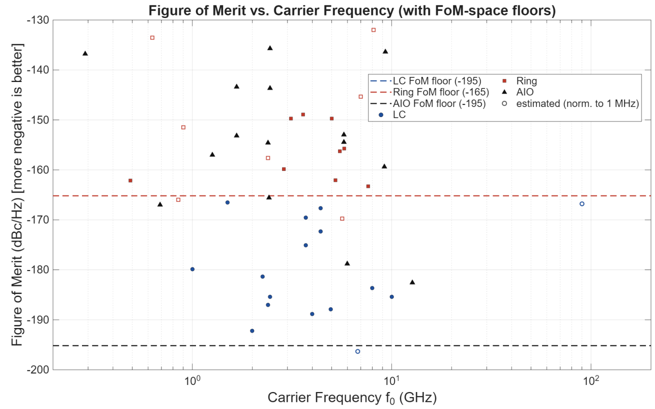

Figure 4: Figure of merit versus carrier frequency. The dashed horizontal lines are the per class minimum FoM floors.

3.3 Trends and Selection

Across publication year (Fig. 5), each family's best-to-date FoM frontier is stable: LC settles near -196 dBc/Hz around 2010, while the ring and active inductor frontiers hold near -170 and -183 dBc/Hz.

4 Conclusion

Selecting the right oscillator for a free-running, crystal-free system requires knowing how far each class can realistically be pushed, and how much of that headroom has already been spent. In this paper we surveyed the LC, ring, and active inductor oscillator classes, and placed 50 published designs, spanning from 2004 to 2025, on common normalized axes of phase noise, power, and figure of merit so that their measured performance could be compared directly.

We found that the three classes fall into distinct, though overlapping, performance brackets with LC defining the low noise edge at a best FoM near -196 dBc/Hz, and the best ring and active inductor designs sitting near -170 and -183 dBc/Hz respectively. Comparing each design against the thermal noise floor of its own class, the best ring oscillators are already within a few dB of their thermal/switching limited floor and they reach it while drawing the

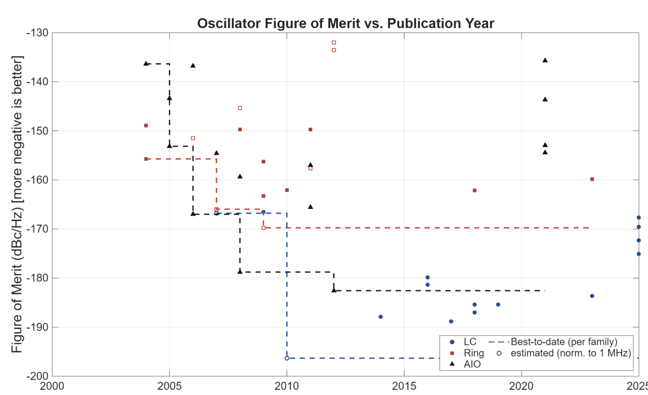

Figure 5: Figure of merit versus publication year. The dashed lines trace the best FoM achieved to date within each family.

most power of the three classes, so there is little room left to improve their phase noise at a given power and frequency without additional filtration techniques. Therefore, LC and active inductor oscillators present the better way forward, by virtue of their quality factor. However, on-chip LC quality factors are themselves limited which makes the active inductor the more compelling choice of the two. The best active inductor designs still fall well short of the resonant floor that LC oscillators approach, likely because the gyrator transistors that synthesize the inductance inject additional colored noise. This leaves the active inductor class as both the least explored and the one with the most headroom remaining, and hence, in our view, the most promising direction for future work on crystal-free oscillators. Resolving the LC and active inductor floors from each design's loaded Q, rather than the fixed factor used here, along with the addition of more active inductor data, are the natural next steps.

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