System-Level Optimization of Cross-Coupled Rectifiers for 3GPP-Compliant Ambient IoT

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Abstract

Radio frequency energy harvesting (RFEH) is essential for battery-free, crystal-free IoT, yet designing rectifiers for ultra-low-voltage (ULV) inputs faces efficiency and transient time challenges. This paper introduces an optimized 2-stage cross-coupled differential (CCD) rectifier in 130 nm CMOS for 868 MHz operation. With a 9.3 mV peak input, the design achieves a steady-state DC output of 1 V across a 5 pF and 1 MΩ parallel load in about 5 μs, reaching a −26 dBm cold-start threshold at the Ambient IoT (A-IoT) node. Our system-level co-design shows that minimizing stages drastically cuts transient charging time, which is critical for crystal-free nodes, without sacrificing detection thresholds. This optimized configuration fulfills the peak power and transient timing specifications for 3GPP Ambient IoT architectures, effectively minimizing operational latency during large-scale network deployments.

CCS Concepts

• **Hardware → Energy harvesting**.

Keywords

Ambient IoT, RF Energy Harvesting, Cross-Coupled Differential Rectifier, 3GPP, Crystal-free IoT, CMOS

1 Introduction

Future IoT sensor networks rely on ambient RF energy harvesting to avoid impractical battery replacements. The 5G ecosystem is adopting ultra-low-complexity A-IoT devices, targeting a 10-trillion-unit market.[4]. Aligned with 3GPP Release 19, the current focus remains on the standardization of "Device 1" for licensed spectrum deployments [1]. These A-IoT nodes are constrained by a 1 μW peak power envelope, leverage passive backscatter modulation, and are designed for indoor operational ranges between 10 and 15 m.

RF-to-DC conversion is challenging because low-power signals produce millivolt-level antenna voltages, far below typical CMOS threshold voltages. Consequently, enabling rectification requires passive amplification or advanced topologies. Two theoretical branches address rectifier threshold constraints. The first uses diode-connected models, with advanced versions accounting for body effects and reverse leakage [3, 8]. The second utilizes cross-coupled differential (CCD) models to dynamically reduce thresholds, minimizing resistance while suppressing leakage [2, 5]. Rather than using dense Power Conversion Efficiency (PCE) models based on Bessel functions or Taylor series, we prioritize rapid transient charging to meet 3GPP Release 19 Ambient IoT duty cycles. Following the system-level linear interface strategy from [7], we apply a simulation-based approach to enhance transient response. The 2-stage CCD rectifier produces a 1 V DC output across a 1 MΩ load, satisfying the target 1 μW power budget at a −26 dBm minimum input sensitivity. With a 5 pF load, it settles from 0 to 99% in 5 μs, enabling storage capacitor scaling up to 33 nF while completing cold-start within a single 33.3 ms 3GPP polling window for rapid duty-cycled energy replenishment.

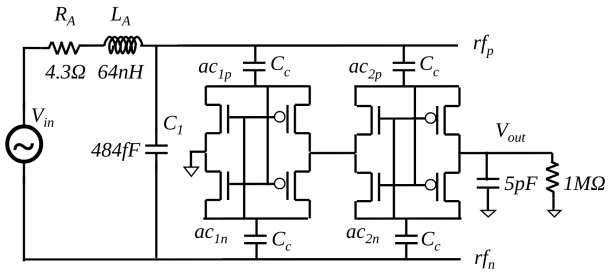
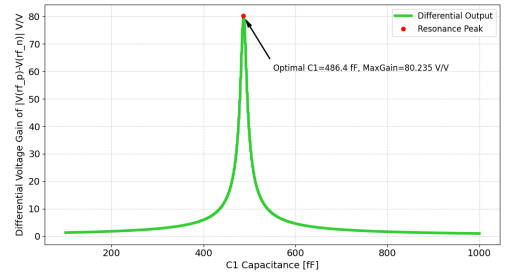


Figure 1: Two-stage RF energy harvester with antenna-rectifier impedance matching scheme.

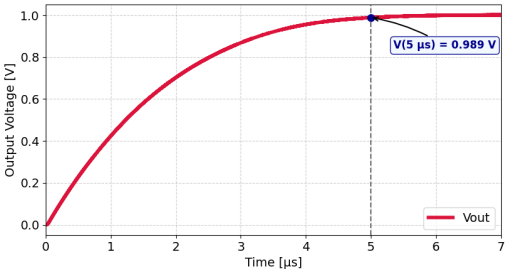
To validate compliance with 3GPP Release 19 Ambient IoT targets, a link budget was evaluated for Topology 1 (gNB) and Topology 2 (UE) at 868 MHz. Governed by Friis transmission principles, under a 35.16 dBm EIRP limit, incident power is −24.06 dBm at 10 m (+1.94 dB margin over the −26 dBm sensitivity) and −27.58 dBm at 15 m, confirming 10-meter cold-start viability. On the uplink (−5 dB reflection efficiency, 100 kHz bandwidth), the backscattered signal reaches the gNB at −82.22 dBm, well above the −109 dBm sensitivity (+26.78 dB margin). For Topology 2, the 23 dBm UE transmit power limit restricts purely RF-powered reads to roughly 3 m. Section 2 examines existing theoretical models, while Section 3 details the optimized 2-stage architecture design methodology.

2 Review of Existing Rectifier Models

Although simplified models suggest output voltage scales linearly with stages, empirical studies show a sub-linear $\sqrt{N}$ dependence due to decreasing input impedance [7]. Diode-connected topologies [8] suffer from three non-linear bottlenecks: parasitic gate-to-substrate capacitances that attenuate AC swing, reverse conduction leakage during negative half-cycles, and body-effect threshold shifts from accumulated DC potential. Using the co-design framework from [7], reducing antenna resistance (R_{A}) to match the rectifier core resistance (R_{rec}) maximizes the passive voltage boost factor $Q_{\mathrm{v}} = \sqrt{R_{\mathrm{rec}}^2 + X_{\mathrm{rec}}^2}/(R_{\mathrm{A}} + R_{\mathrm{rec}})$. As input power increases and the DC voltage stabilizes, the resulting back-voltage limits transistor conduction to brief peaks in the RF cycle. This narrowed conduction angle suppresses fundamental AC current, causing the large-signal rectifier resistance R_{rec} to rise sharply to match the power delivered to the load.



(a) Resonance optimization with C_1 value sweep.



(b) Rectifier DC output voltage charging transient.

Figure 2: Simulation results: (a) Voltage gain resonance peak over C_1 sweep; (b) Rectifier DC output voltage.

3 Proposed Design Methodology

In contrast to complex, multi-stage analytical structures that introduce heavy parasitic penalties [3, 5, 8], the proposed 2-stage rectifier uses an intuitive, system-level design methodology adapted from [7]. The design targets 1 μW DC output across a 1 MΩ load from a 9.3 mV peak RF input at 868 MHz in IHP 130 nm CMOS (Fig. 1), verified via the open-source analog simulator VACASK.

A passive parallel resonant matching network acts as a high-efficiency transformer; at 868 MHz, its high quality factor maximizes the passive voltage boost Q_v, converting the millivolt-level input signal into a high-swing differential AC signal to drive the cross-coupled gates without consuming active power. Rather than relying on traditional scaling, the co-design strategy determines the stage count ($N = 2$) and parametrically optimizes transistor dimensions to balance forward conduction and reverse leakage. Concurrently, the dynamic threshold cancellation scheme doubles the alternating half-cycle gate-to-source voltage (V_{gs}), bypassing internal low-voltage rectification dead-zones. Simply widening transistors (W) to lower R_{on} adds parasitic capacitance (C_{rec}), shunting input reactance (X_{rec}) and dampening the resonant voltage boost (Q_v). Likewise, cascading stages ($N > 2$) increases body-effect threshold shifts (ΔV_{th}) and slows transient charging. Our 2-stage CCD core minimizes parasitic loading, while parallel tuning ($C_1 = 486.4$ fF) preserves a high Q_v (80.2 V/V boost, as shown in Fig. 2a), and coupling capacitors ($C_c = 1$ pF) balance voltage division and silicon area while preventing resonance damping.

As illustrated by the transient response in Fig. 2b, this complete design flow enables rapid charging of the 5 pF capacitive load, delivering 1 μW of power with a 0–99% rise time of just 5 μs. Ultimately, this system-level co-design simplifies modeling while meeting the strict timing and energy constraints of Ambient IoT protocols.

Table 1: Comparison with State-of-the-Art Rectifiers

Metric	[8]	[7]	[6]	[3]	This Work
Topology	10-stage	5-stage	30-stage	5-stage	**2-stage**
Tech. Node	130 nm	90 nm	130 nm	90 nm	**130 nm**
Frequency	900 MHz	868 MHz	915 MHz	900 MHz	**868 MHz**
P_{in}	-25.5 dBm	-27.0 dBm	-31.7 dBm	-23.4 dBm	**-26 dBm**
V_{out}	1 V	1 V	1 V	1 V	**1 V**
R_L	5 MΩ	∞	∞	1 MΩ	**1 MΩ**
Complexity	High	Low	High	Medium	**Low**
Settling	N/A	Fast	Slow	Fast	**Ultra-Fast**

Table 1 demonstrates that sensitivity is driven by passive resonant boosting rather than node scaling or stage cascading. Compared to deep subthreshold harvesters (30–70 stages targeting −31 to −32 dBm [6]) that trade off startup speed due to parasitic accumulation, body-effect shifts, and reverse leakage, our 2-stage core achieves a 5 μs settling time under an active 1 μW load (1 MΩ). This corresponds to an exceptionally low cold-start latency that secures a large amount of active window availability for data transmission within short 3GPP polling windows (33.3 ms). Furthermore, sub-90 nm nodes fail to resolve ULV bottlenecks as higher gate leakage (I_{off}) increases reverse conduction losses (P_{REV}), confirming topology simplification and resonant co-design as key drivers.

4 Conclusion

This paper demonstrated a 2-stage CCD RF rectifier for crystal-free Ambient IoT nodes achieving −26 dBm sensitivity and a 5 μs transient settling time at 868 MHz. Link budget analysis validates 10-meter 3GPP Release 19 Device 1 operation with a +1.94 dB margin. Extending coverage beyond 10 m will require directional interrogator antennas ($\geq$ 1.58 dBi), migrating to licensed 5G cellular bands, or improving the design's sensitivity below −27.58 dBm.

Acknowledgments

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References

[1] 3GPP. 2026. *Technical Specification Group Services and System Aspects Release 19 Description; Summary of Rel-19 Work Items (Release 19).* Technical Report TR 21.919, Version 2.0.0. 3GPP.

[2] Shih-En Chen, Yi-Chung Lin, and Kuang-Wei Cheng. 2022. A High Sensitivity RF Energy Harvester with Dynamic Body-Biasing CMOS Rectifier. *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)* (2022), 308–312.

[3] L. G. de Carli, Y. Juppa, A. J. Cardoso, C. Galup-Montoro, and M. C. Schneider. 2015. Maximizing the Power Conversion Efficiency of Ultra-Low-Voltage CMOS Multi-Stage Rectifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers* 62, 4 (April 2015), 967–975.

[4] Y. Kim. 2026. Challenges and Advances in Ambient IoT within 3GPP. *IEEE Communications Magazine* 64, 1 (January 2026), 182–188.

[5] S. M. Noghabaei, R. L. Radin, Y. Savaria, and M. Sawan. 2022. A High-Sensitivity Wide Input-Power-Range Ultra-Low-Power RF Energy Harvester for IoT Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers* 69, 1 (January 2022), 440–451.

[6] Seunghyun Oh and David D. Wentzloff. 2012. A -32dBm sensitivity RF power harvester in 130nm CMOS. *2012 IEEE Radio Frequency Integrated Circuits Symposium* (2012), 483–486.

[7] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn. 2014. Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters. *IEEE Journal of Solid-State Circuits* 49, 3 (March 2014), 622–634.

[8] J. Yi, W. H. Ki, and C. Y. Tsui. 2007. Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers* 54, 1 (January 2007), 153–166.