Towards a Physical-Layer Digital Twin for Backscatter Systems

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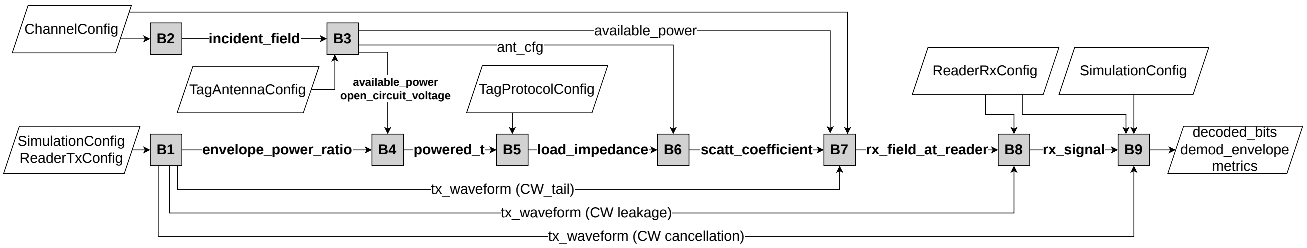

Figure 1: Block diagram. Python source code available: bitbucket.org/wineuoc/rfid-phy-digitaltwin.

Abstract

Extending digital functionality to everyday products without increasing their cost, material complexity, or environmental burden requires ultra-low-impact communication architectures. Crystal-free backscatter is promising in the Ambient-IoT (A-IoT) context, particularly for devices implemented on biodegradable or organic substrates, but its PHY design is tightly constrained by nonidealities inherent to low-cost implementations. Evaluating the resulting interactions among waveform, modulation and coding (WMC) and hardware nonidealities exposes a gap between network-level abstractions and computationally intensive circuit-level models. This paper introduces a discrete-time complex-baseband link-level simulator that models reader excitation, nonlinear energy harvesting, impedance modulation, backscatter propagation, and reader-side detection. The framework provides a configurable basis for studying backscatter communication strategies under hardware and channel impairments.

CCS Concepts

• **Networks** → **Link-layer protocols**; **Network protocol design**;
• **Computing methodologies** → **Simulation tools**.

Keywords

Backscatter Communication, Digital Twin, Physical Layer Simulation

1 Introduction

Extending digital functionality to everyday products without compromising their affordability, recyclability, or environmental footprint requires ultra-low-impact communication architectures. Crystal-free backscatter is a promising approach. By eliminating active RF oscillators, these backscatter devices achieve the near-zero power profiles essential for ubiquitous deployment within A-IoT [5].

Designing the PHY layer for emerging biodegradable or organic hardware introduces unique challenges, as severe power and logic limits deeply intertwine WMC choices with hardware constraints. For instance, non-linear RF-to-DC harvesting efficiency depends heavily on waveform shape, while a massive SFO up to 10^5 ppm severely impacts reliability, strictly dictating viable WMC schemes [2, 4].

Evaluating these coupled effects exposes a methodological gap. Network-level simulators (e.g., NS-3) excel at MAC resolution but abstract away low-level PHY dynamics, employing idealized linear harvesting models that miss non-linearities and monostatic self-jamming [1, 2]. Conversely, circuit-level RF simulators (e.g., SPICE) capture non-linear diode dynamics but cannot scale to simulate full protocol handshakes, multi-path fading, or end-to-end BER over millions of samples [2].

To bridge this divide, we introduce a discrete-time, complex-baseband Link-Level Digital Twin Simulator for the Gaia Pathfinder project. By jointly modeling reader excitation, non-linear harvesting, impedance modulation, and coherent demodulation, it accurately merges electromagnetic physics with digital signal processing. This provides a scalable platform to rigorously evaluate WMC strategies under the severe hardware impairments inherent to crystal-free systems.

2 Digital Twin Simulator

While the digital twin's architecture is highly flexible, its foundational implementation models the ISO 18000-6C (EPCglobal Gen 2) physical layer. This mature standard serves as a strictly verifiable baseline to ground-truth the underlying physics engine, ensuring theoretical correctness and reproducibility before exploring custom WMC schemes. All underlying mathematical models, as RF propagation and backscatter mechanics, are strictly grounded in the fundamental equations detailed by [3].

*All authors are with the Wireless Networks Research Lab, Universitat Oberta de Catalunya, Spain. This work is funded by the "GAIA" project, having received funding from the European Union, the European Innovation Council and SMEs Executive Agency under the grand agreement No. 101256099. Professor Xavier Vilajosana is supported by an ICREA Academia grant.

Table 1: Functional Summary of the 9-Block Pipeline

Block	Functional Description
B1. Reader Excitation	Synthesizes complex baseband reader waveforms, generates PIE symbols, and injects oscillator phase noise.
B2. Forward Channel	Models Line-of-Sight propagation and complex Fresnel ground reflections to compute incident power density.
B3. Tag Antenna	Converts the incident electromagnetic field into a Thévénin equivalent circuit open-circuit voltage.
B4. Non-Linear Harvesting	Simulates dynamic Dickson charge pump rectification efficiency and reservoir capacitor RC smoothing.
B5. Protocol & Mod	Maps uplink response bits to an FM0/Miller antenna load impedance trajectory, applying unpowered masks.
B6. Differential RCS	Translates time-varying load states into instantaneous structural and mismatch Radar Cross-Section bounds.
B7. Reverse Channel	Executes inverse propagation of the backscattered wave back to the reader receiver aperture.
B8. Reader Frontend	Introduces monostatic carrier leakage (self-jamming), thermal noise figure penalties, and AWGN corruption.
B9. Demod & Eval	Performs leakage cancellation, dynamic rolling-median envelope slicing, and end-to-end BER extraction.

Table 2: Simulation Classes and Key Parameters

Class	Key Parameters
Reader TX	Carrier frequency, EIRP, Antenna gain, Waveform (CW/Inventory), Modulation (PR-ASK/DSB-ASK), Tari, Phase noise floor
Channel	Model (Free-space/Two-ray), Floor refractive index
Tag Antenna	Polarization mismatch, Input capacitance, Complex impedance, Gain
Tag Harvester	Dickson stages, Diode turn-on voltage, Load resistance, Storage capacitance, Chip boot threshold
Protocol	Coding scheme (FM0/Miller), Subcarrier index
Reader RX	Noise figure, Receive gain, Carrier leakage, Slicer mode

2.1 Pipeline Architecture

The Python-based simulator is structured as a sequential, nine-block pipeline bridging electromagnetic propagation, non-linear circuit operations, and digital signal processing. The blocks are depicted in Figure 1. Conceptually, this pipeline spans three primary phases: the forward link (reader excitation and multi-path propagation), tag physics (energy harvesting and impedance modulation), and the reverse link (backscatter propagation and coherent demodulation). A detailed functional breakdown of each block within this sequence is provided in Table 1. Key parameters are listed in Table 2.

2.2 Time-Domain Simulation Mechanics

The digital twin employs a discrete-time, complex-baseband architecture via a high-resolution global sample grid. The carrier frequency is decoupled from the time-domain arrays, acting strictly as a scalar for spatial path-loss and phase shifts, while the arrays track the modulation envelope's amplitude and phase.

Operating sequentially to reflect half-duplex backscatter, this array-driven approach intrinsically captures transient physical effects. The pipeline initializes with FIR pulse-shaping and $1/f^2$ oscillator phase noise injection. The harvesting block then evaluates instantaneous rectification efficiency, applying a single-pole IIR filter to simulate capacitor hold-up times and predict mid-reply brownouts. Subsequently, the protocol block maps the available power to an FM0/Miller load-impedance trajectory, forcing a conjugate-match rest state during unpowered samples. Finally, the reverse link injects AWGN and coherent carrier leakage, executing symbol-boundary detection via dynamic rolling-median thresholding.

2.3 Performance Metrics and Outputs

The simulator yields physical-layer telemetry, extracting analytical evaluation metrics from the complex baseband. The primary output is the end-to-end BER, which can be evaluated continuously by sweeping system parameters (Table 2) to identify precise forward and reverse link cutoff boundaries. Additionally, the simulator extracts the ACPR via FFT-based PSD analysis to verify compliance with dense-interrogator spectral masks. Intermediate telemetry such as instantaneous harvested DC power, dynamic leakage-to-signal ratios, and raw receiver envelopes is exposed for in-depth link-budget analysis.

3 Conclusion & Future Work

By bridging the gap between hardware constraints and protocol design, the proposed digital twin offers several practical applications for A-IoT research. Specifically, the simulator provides a robust platform for establishing PHY-layer baselines, conducting coupled WMC evaluation, executing holistic constraint integration, performing environmental resilience analysis, and accelerating DSP algorithm prototyping.

A primary advantage of strictly implementing the ISO 18000-6C standard is the ability to ground-truth the digital twin. Immediate future work involves validating the simulator's predictive accuracy—such as exact forward and reverse link cutoff boundaries—by comparing its telemetry against physical measurements from commercial-off-the-shelf (COTS) UHF RFID readers and tags under controlled real-world conditions. Beyond the current deterministic Two-Ray ground-reflection channel model, we plan to incorporate stochastic multipath fading to evaluate packet error rates in highly scattered environments. To accelerate these efforts, we plan to open-source the framework and actively seek community collaboration.

Future work focuses on empirical validation against COTS UHF RFID readers and expanding the platform into a multi-fidelity Physical-Layer Digital Twin. By integrating SPICE-level circuit models (e.g., CMOS rectifiers, PMU cold-start dynamics) block-by-block, the simulator transitions from an analytical link-level tool into a true digital twin mirroring real silicon. Additionally, beyond the current deterministic Two-Ray ground-reflection engine, we will incorporate stochastic multipath fading and support ambient OFDM sources, higher-order trajectories (16-QAM), and crystal-free SFO recovery.

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