A Tool for On-Chip Inductor Design Using Geometric Programming

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Abstract

On-Chip inductors are core components in many RF circuits including oscillators, LNAs, mixers and filters, which makes their sizing a fundamental problem for crystal-free radios. Integrating inductors directly onto silicon using open-source process design kits (PDKs) is difficult since they lack the appropriate tools, forcing designers to rely on commercial EDA software or use slow iterative approaches that do not necessarily yield the highest possible Q-factor for a given operating frequency and inductance value. This paper presents an open-source tool capable of optimizing inductor geometry without the need of EM simulation. Global optimality is guaranteed by the convex structure of the geometric programming (GP) formulation. Differential inductors, one-port inductors and LC tanks can be designed with this tool, enabling direct use in oscillator and LNA design. Results have been validated using AWS Palace on the IHP SG13G2 process.

CCS Concepts

• **Hardware → Integrated circuits**; *Wireless devices*; *Networking hardware*; Modeling and parameter extraction; *Software tools for EDA*.

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1 Introduction

Open-source IC design flows have generated great interest in recent years because they enable research and development without the elevated costs of commercial flows, as well as promoting collaboration between research groups and greatly increasing the amount of available educational tools. Unfortunately, no open-source tools exist for optimal inductor design, making RF circuits difficult to implement without commercial EDA. Current solutions to this problem are limited to iterative approaches which require significant computational effort and time to generate a single valid inductor geometry without ensuring the optimality of the solution.

This paper presents an open-source implementation of the geometric programming approach first proposed by Hershenson et al. [3] for inductor circuits. This approach allows the designer to obtain the optimal geometry for an inductor with a given target inductance value and operating frequency, while also taking into account self-resonance constraints, maximum silicon area, substrate losses and other significant factors that impact the final Q-factor. Because GP problems can be made convex by a change of variables [2], the solution found by optimizing the convex model is guaranteed to be the optimal solution. GP allows designing an inductor without the need for electromagnetic (EM) simulation. EM simulation is often slow and resource-intensive, which makes it more suitable for verification rather than design. The proposed workflow uses the GP model to generate the best possible inductor geometry and EM simulations to verify the model matches the specifications.

2 Background and Related Work

In [1], Ashby et al. present an equivalent pi-model for complementary bipolar processes. Their main contribution was the inclusion of substrate capacitance and resistance, which makes the model better match the measurements. This model was used in [13] to compare ASITIC simulations to measurements and in [19] each component was assigned an equation in terms of geometry and process variables. This equations include data-fitted parameters which ensure the pi-model matches the measurements and mask effects like fringing and inter-turn capacitance.

In [11], authors derive a monomial expression for inductance using only geometry parameters. This monomial fit was used in [3] to generate inductors using a GP model to find the highest Q factor possible for a given inductance value. It's important to note that for the model presented in [3], only inductance was validated against real measurements. Furthermore, EM simulations show that shunt capacitance and resistance, as well as series capacitance, don't match the values predicted by the model, showing that new equations must be derived in order to use the pi equivalent for design rather than analysis.

The design space for a planar inductor is defined by the number of turns n, the conductor width w, the spacing between turns s, and the outer diameter d_{out}. All other geometry parameters can be derived from these four values. Conductor thickness is considered to be fixed so it will not be included as a design variable.

An initial solution for an inductor geometry that matches a certain inductance value can be derived from a modified version of

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Wheeler's formula[11]

$$L \approx K_1 \mu_0 \frac{n^2 (d_{\text{out}} + d_{\text{in}})/2}{1 + K_2 \rho}, \tag{1}$$

where K_1 and K_2 depend on the inductor shape and ρ is the fill factor, defined as $\rho = (d_{\text{out}} - d_{\text{in}})(d_{\text{out}} + d_{\text{in}})$. By fixing n and d_{out}, for example, the required inner diameter can be obtained and thus the turn width and separation can be obtained, however, there is no guarantee that this solution produces an acceptable Q-factor. This initial geometry can be later refined iteratively by modifying one of the variables, running an EM simulation and comparing the obtained Q-factors. The amount of iterations required to obtain a certain Q-factor value depends on the initial guess, but there's no way of making an educated guess without first running a series of EM simulations. Sweeping all four design variables requires a significant number of EM simulations and compute power, making the process of circuit design slow and demanding. An iterative workflow for IHP SG13G2 is available as an example of the `gds2palace` tool [12].

3 Target Geometry and Proposed Model

The target geometry for this work is an symmetrical octagonal inductor like the one shown in figure 1. This kind of inductors are

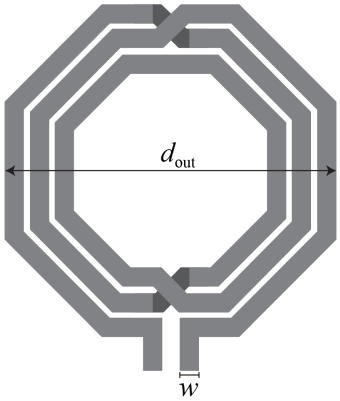

Figure 1: Symmetrical octagonal inductor with $N = 3$.

used in differentially-driven circuits like oscillators. Because the circuits in [1] and [19] are based on spiral inductors, the model must be adjusted to match the target.

The lumped element model used [19] is shown in Figure 2.

Series capacitance is composed of inter-turn capacitance underpass capacitance, while shunt capacitance and resistance depend on substrate and oxide characteristics.

3.1 Inter-turn Capacitance

Inter-turn capacitance in symmetrical inductors is much greater than in spiral geometries [15], owing to the fact that adjacent turns have a bigger voltage difference.

In order to obtain the equivalent capacitance we first start by assuming a linear voltage profile between both terminals, meaning that when driven differentially, one of the ports is at $V_{\text{in}}/2$ while the second port is held at $-V_{\text{in}}/2$. From this linear voltage profile,

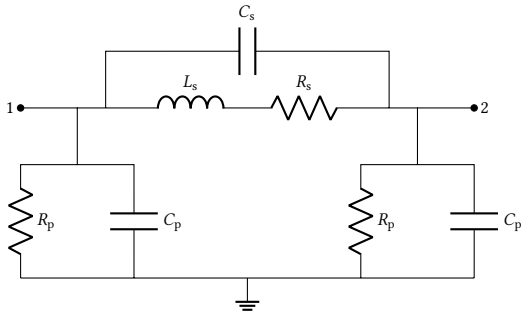

Figure 2: Inductor lumped element model.

we can obtain the voltage difference in the gaps formed by adjacent turns from

$$V_k = \frac{N - k}{N} V_{\text{in}}, \tag{2}$$

where k is the gap index and N is the number of turns. The outermost gap has index k and the innermost gap has index $N - 1$. This means the energy stored in the k-th gap is given by the expression

$$E_k = \frac{1}{2} \left(\frac{N - k}{N} V_{\text{in}} \right)^2 C_k, \tag{3}$$

where C_k is the capacitance of that gap. Capacitance C_k is a function of gap length l_k, which can be expressed as

$$l_k = 8 \tan \frac{\pi}{8} [d_{\text{out}} - w - (2k - 1)(w + s)], \tag{4}$$

and capacitance per length $C_l = \epsilon(t/s + \delta)$, where δ is a fringe factor modeled. By summing individual energy contributions, we can express the total energy stored in the inter-turn spacings as

$$E_{\text{tot}} = \sum_{k=1}^{N-1} \frac{1}{2} \left(\frac{N - k}{N} V_{\text{in}} \right)^2 C_k = \frac{1}{2} V_{\text{in}}^2 C_{\text{it}}, \tag{5}$$

where C_{it} is the equivalent capacitance. By carrying out the sum, we arrive at

$$C_{\text{it}} = \left(\frac{N - 1}{6N} \right) C_l 8 \tan \frac{\pi}{8} \times \left[(2N - 1)(d_{\text{out}} - w) - (N^2 - N + 1)(w + s) \right]. \tag{6}$$

The fringe factor δ in C_l is modeled as

$$\delta = 0.36 \times \left(\frac{w}{w + s} \right), \tag{7}$$

where $\frac{w}{w+s}$ corresponds to the fill factor of the inter-turn gap. Note that this expression was obtained by fitting a large number of inductors simulated in Palace[5] rather than analytically. We found that the formula in 6 is accurate as it presents a median error of 3% with around 14% root-mean-square (RMS) error scatter when compared to the simulations in the design domain.

3.2 Underpass Capacitance

In order to keep the symmetry of the inductor, subsequent turns must be interleaved, which results in $N - 1$ underpasses where a w^2 area is enclosed by different turns. Since we assumed a linear voltage profile, we can obtain the voltage difference between the

enclosing turns and so the energy stored at each underpass. For the j-th underpass we have

$$V_j = \left(\frac{N-j}{N}\right) V_{\text{in}} \qquad E_j = \frac{1}{2}\left(\frac{N-j}{N} V_{\text{in}}\right)^2 C_{\text{enc}}, \tag{8}$$

where C_{enc} is the capacitance of the enclosed w^2 area

$$C_{\text{enc}} = \frac{\epsilon_{\text{ox}}}{t_{\text{via}}} w^2. \tag{9}$$

Since all underpasses are equal in area, the total capacitance is $C_{\text{tot}} = (N-1)C_{\text{enc}}$, so we can obtain the equivalent capacitance from the energy formula directly

$$E_{\text{tot}} = \sum_{j=1}^{N-1} \frac{1}{2}\left(\frac{N-j}{N} V_{\text{in}}\right)^2 C_{\text{enc}} \tag{10}$$

$$E_{\text{tot}} = \frac{1}{2} V_{\text{in}}^2 \frac{(N-1)(2N-1)}{6N} \frac{C_{\text{tot}}}{N-1} = \frac{1}{2} V_{\text{in}}^2 C_{\text{up}} \tag{11}$$

$$\Rightarrow C_{\text{up}} = \frac{(N-1)(2N-1)}{6N} \frac{\epsilon_{\text{ox}}}{t_{\text{via}}} w^2. \tag{12}$$

3.3 Series Resistance

The series resistance of the inductor depends on the conductivity σ_m of the metal layer used to draw the coil and the operating frequency f. Using the model proposed in [9] for current crowding effects, the series resistance for this inductor geometry can be approximated by

$$R_{\text{series}} = \frac{l}{\sigma w \delta_{\text{skin}}(1 - e^{-t/\delta_{\text{skin}}})} \left[1 + \frac{1}{10}\left(\frac{f}{f_{\text{crit}}}\right)^2\right], \tag{13}$$

where $\delta_{\text{skin}} = \sqrt{2/(2\pi f \mu_0 \sigma_m)}$ is the skin depth and f_{crit} is the frequency at which current crowding starts to affect the effective resistance value. This frequency can be obtained by the approximation

$$f_{\text{crit}} = \frac{3.1}{2\pi\mu_0} \frac{w+s}{w^2} \frac{1}{\sigma_m t_m}, \tag{14}$$

where t_m is the metal thickness.

Series resistance has a big impact on the inductor Q factor, so it's important to note that this approximations will introduce some error to the GP model. Since the presented equations tend to overestimate R_{series}, the generated geometries may exhibit a higher Q factor than predicted. This effect can be beneficial when designing inductors for oscillator circuits, but will make applications like LC tanks more difficult to design. The impact of the approximations of R_{series} in self resonance frequency prediction (SRF) is negligible. Standard coupled-microstrip theory [4] gives C_{even} as the response of the neighboring segments when both conductors are set to the same potential, which in this case is only a mathematical device to obtain the coefficient.

3.4 Oxide Capacitance

Oxide capacitance can be expressed as [17]

$$C_{\text{ox}} = \frac{1}{2}(C_A + C_P), \tag{15}$$

where C_A is the area capacitance that can be estimated as

$$C_A = A \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}, \tag{16}$$

and C_P is the fringing perimeter capacitance

$$C_P = P C_{\text{SP}}, \tag{17}$$

where P is the total perimeter of the octagonal inductor and C_{SP} is the specific fringing capacitance per unit length. This value can be obtained analytically by treating the N turns as a single bundle of width $W_{\text{bun}} = Nw + (N-1)s$ and evaluating the isolated-microstrip fringing capacitance of that bundle:

$$C_{\text{SP}} = \frac{1}{2}\left[C_{\text{iso}}(W_{\text{bun}}) - \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} W_{\text{bun}}\right], \tag{18}$$

where $C_{\text{iso}} = \epsilon_{\text{eff}} C_{\text{air}}$ is the standard closed-form isolated-microstrip capacitance [6], with the effective permittivity corrected for the passivation layer above the metal in SG13G2 [16, 18].

3.5 Substrate Capacitance

Two physical mechanism contribute to substrate capacitance C_{sub}: a parallel-plate term set by the metal traces and the substrate thickness and a self-capacitance term from field lines that fringe from the outer edge of the winding and reach the ground plane without passing under the coil. The latter term dominates because the backside ground sits roughly a coil radius away, putting the winding closer to an isolated-conductor self-capacitance structure than a simple overlap capacitor.

From [7], the self-capacitance of an isolated conductor scales linearly with its characteristic radius. This suggests that we can write the self-capacitance term as $\beta_{\text{sub}} \cdot a_{\text{self}}$, with $a_{\text{self}} = \sqrt{A_{\text{foot}}/\pi}$ the equivalent radius of the winding's outer footprint area $A_{\text{foot}} = 8(\sqrt{2}-1)(d_{\text{out}}/2)^2$.

Since there's no closed form equation for an octagonal ring above a grounded dielectric slab, we are forced to find the rim term coefficient β_{sub} empirically

$$C_{\text{si}} = \beta_{\text{sub}} \cdot a_{\text{self}} + \frac{\epsilon_{\text{si}}\epsilon_0}{t_{\text{sub}}} A_{\text{metal}}, \tag{19}$$

where $A_{\text{metal}} = lw$ is the coil total metal area and $\beta_{\text{sub}} = 3.78 \times 10^{-10}\,\text{F}\,\text{m}^{-1}$ was extracted from Palace simulations which didn't include inductors, only planar surfaces. Cross-validating this quantity against a large data set of inductors, we find that equation 19 reproduces the EM-extracted C_{si} with a median error of 2% and an RMS scatter of 13.6%.

C_{si} is exact and monomial in both terms already, so no monomial fit is required to use it in the GP model.

3.6 Substrate Resistance

Substrate resistance R_{si} can be obtained from C_{si} using the dielectric relaxation time constant τ. Note that each of the two capacitance components has its own associated relaxation time and that the two conduction paths combine as parallel admittances

$$R_{\text{si}} = \frac{1}{G_{\text{si}}}, \qquad G_{\text{si}} = \frac{(\epsilon_{\text{si}}\epsilon_0/t_{\text{sub}})A_{\text{metal}}}{\tau_{\text{si}}} + \frac{\beta \cdot a_{\text{self}}}{\tau_{\text{self}}}. \tag{20}$$

The first term corresponds to the parallel-plate capacitance between the metal traces and the ground and it uses the bulk material relaxation time $\tau_{\text{si}} = \epsilon_{\text{si}}/\sigma_{\text{sub}} = 52.7\,\text{ps}$, determined entirely by the process. On the other hand, the relaxation time of the self capacitance term, τ_{self} is not a material constant as it depends on the current spread along the lossy substrate. By extracting this constant

from a large dataset of coil simulations we find that $\tau_{\text{self}} = 68.2$ ps makes R_{si} match the EM-extracted values with a median error of 2% and a RMS scatter of 13.3%, matching the accuracy of C_{si} a expected.

4 Geometric Programming Model

4.1 GP-Compatible Expressions

Since the equations in the previous section are not monomials or posynomials, they must be adapted to enter a GP model. Series inductance can be well approximated by the monomial [11]

$$L_s = \beta d_{\text{out}}^{\alpha_1} w^{\alpha_2} d_{\text{avg}}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{21}$$

where coefficients β and α_i are layout dependent and must be fitted. In [11], coefficients for an octagonal spiral inductor are presented, but since our target geometry is a symmetric inductor, the coefficients must be modified. By simulating a large number of inductors and fitting the coefficients using a simple least-square fit, we found that retaining the α_i coefficients presented in [11] and adjusting the magnitude coefficient to be $\beta = 1.222 \times 10^{-}3$ resulted in a mean error of only 0.51% on a 98 coil dataset, with a RMS error of 9.46%.

In order to convert equation 6 into a GP-compatible monomial, we first use two log-log least-squares regression approach to fit a monomial to the exact closed form. By sweeping C_l over the PDK allowable values of w and s and solving $\log C_l = \log A + p_w \log w + p_s \log s$ by ordinary least squares, we find

$$C_l(w, s) \approx 7.2962 \times 10^{-11} \cdot w^{0.16420} \cdot s^{-0.78702}, \tag{22}$$

where C_l is in $\mathrm{F\,m^{-1}}$, w and s in µm. Now we fit the inter-turn capacitance following a similar method to find

$$C_{\text{it}} \approx 8 \tan \frac{\pi}{8} \left[A_l, w^{p_w} s^{p_s}\right] \times \left[A_d N^{p_d} d_{avg} + A_w N^{p'_w} w + A_s N^{p'_s} s\right]. \tag{23}$$

The coefficients for this C_{it} fit are shown in table 1.

Table 1: Coefficients for monomial inter-turn capacitance expression

A_l	p_w	p_s	A_d	p_d
7.2962×10^{-11}	0.1642	-0.78702	0.13344	1.35062
A_w	p'_w	A_s	p'_s	
0.016814	2.91993	0.073753	2.32659	

Since the underpass capacitance is already a monomial in w, only the $(N-1)(2N-1)/(6N)$ must be fitted to turn it into a GP compatible expression. The log-log least-squares approach results in

$$C_{\text{up}} \approx \frac{\epsilon_{\text{ox}}}{t_{\text{via}}} A_{\text{up}} N^{p_{\text{up}}} w^2, \tag{24}$$

where t_{via} is the spacing between the coil and the underpass (the same thickness a via connecting the two would have) and the coefficients are $A_{\text{up}} = 0.134$ and $p_{\text{up}} = 1.348$. The legalization reproduces the exact turn factor to within −2% to +6% over $N \in [3, 9]$. The approximation should not be used for $N \leq 2$ since the monomial fit collapses.

For the oxide capacitance, since C_A is already a monomial in d_{avg}, N, w, and s, only the specific perimeter capacitance $C_{\text{SP}}(W_{\text{bun}})$ requires legalization. A log-log least-squares fit over the PDK-allowable range of W_{bun} gives

$$C_{\text{SP}} \approx A_{\text{sp}} W_{\text{bun}}^{p_{\text{sp}}}, \tag{25}$$

with $A_{\text{sp}} = 1.6842 \times 10^{-11}\,\mathrm{F\,m^{-1}}$, W_{bun} in µm and $p_{\text{sp}} = 0.08904$, reproducing the exact $C_{\text{SP}}(W_{\text{bun}})$ to within 1.8% over the whole design range. Combining and simplifying, the full monomial expression for the oxide capacitance is

$$C_{\text{ox}} \approx 4 \tan \frac{\pi}{8} d_{\text{avg}} \left[\frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} N(w+s) + 2A_{\text{sp}}\big(Nw + (N-1)s\big)^{p_{\text{sp}}}\right]. \tag{26}$$

4.2 Quality Factor

In order to correctly model the Q factor, we first need to define the shunt capacitance C_p and the shunt resistance R_p from our model parameters. From [3], we can express the shunt resistance as

$$R_p = \frac{1 + [\omega R_{\text{si}}(C_{\text{si}} + C_{\text{ox}})]^2}{\omega^2 R_{\text{si}} C_{\text{ox}}^2}, \tag{27}$$

but since our model no longer has monomial expressions for each of these quantities (C_{ox} is now a posynomial), R_p can't enter the GP model directly. This same issue occurs in the expression for the shunt capacitance

$$C_p = \frac{C_{\text{ox}} + \omega^2 R_{\text{si}}^2 (C_{\text{si}} + C_{\text{ox}}) C_{\text{si}} C_{\text{ox}}}{1 + [\omega R_{\text{si}}(C_{\text{si}} + C_{\text{ox}})]^2}. \tag{28}$$

In order to keep the model GP-compatible an iterative approach was devised; the ratio of R_p and R_s is expressed as a dimensionless variable κ that gets seeded at the start of the program and frozen at each iteration. Once the GP model is solved with the frozen κ_R value, the exact for R_p is obtained using equation 27 and κ_R updated for the next solve. A similar approach is used for C_p, with κ_C being the ratio between C_p and C_{ox}. Once both ratios converge to a configurable threshold, the resulting geometry is presented as the solution.

With R_p and C_p available at each iteration, the Q factor can be obtained as [3]

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{2R_p \left(1 - \frac{R_s^2 \frac{C_p + 2C_s}{2}}{L_s} - \omega^2 L_s \frac{C_p + 2C_s}{2}\right)}{2R_p + \left[\left(\frac{L_s \omega}{R_s}\right)^2 + 1\right] R_s}. \tag{29}$$

4.3 Design Problem and Constraints

The design problem for this model is to find the geometry which gives the highest possible Q factor value for a specific target inductance L_{req}. Since equation 29 is not a posynomial and so it can't enter the GP model directly, we use the following inequality [3] as a constraint

$$\frac{Q_{\min} R_s}{\omega L_s 2R_p} \left[2R_p + \frac{(\omega L_s)^2}{R_s} + R_s\right] + \frac{R_s^2 (C_p + 2C_s)}{L_s} + \omega^2 L_s (C_p + 2C_s) \leq 1. \tag{30}$$

In a similar manner, the minimum SRF can be set by the constraint [3]

$$\omega_{\mathrm{sr,min}}^{s} L_s (C_p + 2C_s) + \frac{R_s^2 (C_p + 2C_s)}{L_s} \leq 1, \tag{31}$$

which also allows us to maximize SRF if $\omega_{\mathrm{sr,min}}$ is used as the target function.

The basic design problem for a maximum Q-factor inductor can be formulated as

$$\begin{aligned} &\text{maximize} && Q_{\min} \\ &\text{subject to} && Q \geq Q_{\min} \\ &&& L = L_{\mathrm{req}} \end{aligned} \tag{32}$$

Additional constraints can be added to the optimization problem easily. This allows for the PDK fabrication constraints to be enforced by the optimizer or an area constraint added to prevent huge coils.

5 Simulation Results

A set of 20 inductor geometries was generated with this tool, with values ranging from 1 nH to 20 nH, and then simulated using Palace [5]. Table 2 shows the dimensions obtained by the GP model and the predicted SRF and Q factor values.

Table 2: Maximum Q factor geometries by inductance

L (nH)	N	w (µm)	s (µm)	d_{out} (µm)	SRF (GHz)	Q
1	2	28.00	2.00	262.8	24.44	13.77
2	3	28.00	2.00	305.4	13.64	15.65
3	3	28.00	2.00	371.0	9.96	15.55
4	3	28.00	2.24	433.5	8.07	14.16
5	4	27.96	2.87	424.0	6.84	12.53
6	4	23.63	3.15	430.9	6.43	11.13
7	5	19.07	3.34	384.6	6.04	10.04
8	5	16.75	3.55	389.0	5.75	9.10
9	5	14.86	3.76	395.5	5.50	8.26
10	6	12.67	3.86	359.5	5.22	7.56
11	6	11.46	4.04	363.9	5.04	6.93
12	6	10.41	4.21	369.1	4.87	6.36
13	6	9.50	4.37	375.0	4.71	5.83
14	7	8.39	4.43	345.0	4.51	5.36
15	7	7.73	4.57	349.2	4.38	4.94
16	7	7.14	4.71	353.8	4.27	4.55
17	7	6.61	4.84	358.7	4.16	4.19
18	7	6.13	4.97	363.8	4.06	3.85
19	7	5.69	5.09	369.0	3.96	3.54
20	7	5.28	5.22	374.4	3.87	3.25

Figure 3 shows the comparison between the target inductance for the GP mode and the measured inductance from EM simulation. We note that the GP model closely tracks the EM simulations, with the error becoming greater at higher inductance values. Also, this plot shows the first two data points being far off from the GP predicted value with the 1 nH coil having a 64.9% error with respect to the EM measurements.

In Figure 4 we can see a comparison between the predicted and measured Q factor and in Figure 5 the SRF comparison for each coil,

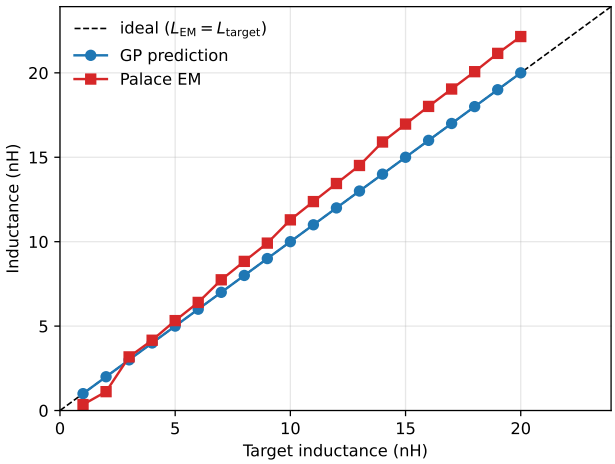

Figure 3: Predicted and measured inductance per coil.

showing that the first two coils exhibit anomalous Q factor values and have an SRF value outside the frequency sweep range. Apart from these two data points, we see the Q factor is under predicted and has a non-uniform error profile while the SRF prediction is close to the EM-extracted values, with an almost constant error of around 25% for coils over 8 nH.

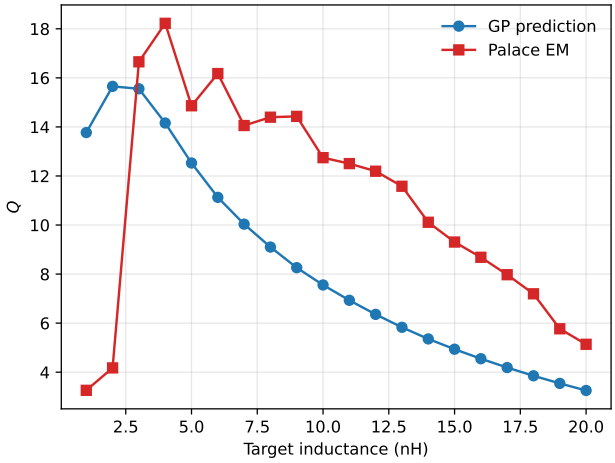

Figure 4: Predicted and measured Q factor per coil.

6 Future Work

6.1 Optimization Techniques

While geometric programming approaches offer a global optimum, they depend on the underlying model being expressed in posynomial form. This limitation introduces additional error to the model, making the solution unreliable in some cases where the monomial approximation is far from the full expression. Recent developments in more complex optimization techniques such as particle swarm

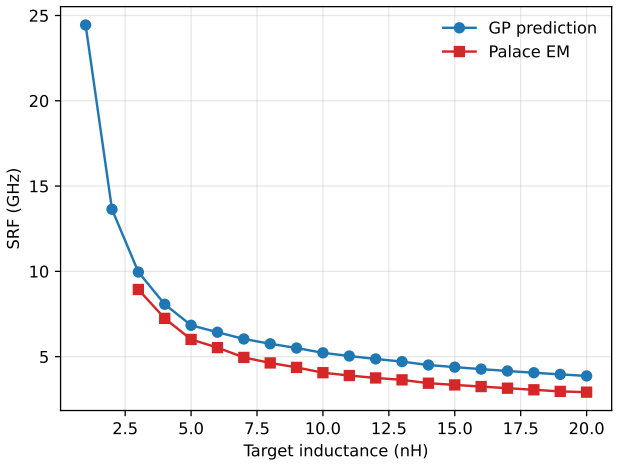

Figure 5: Predicted and measured and SRF per coil.

optimization (PSO) [10, 14] might suggest that the full model presented in section 3 can be used to find the highest feasible Q factor for a given inductance value.

6.2 Patterned Ground Shields and Guard Rings

This work focuses on isolated inductors, meaning the only component included in the EM simulations is the coil. This is of course not realistic as a practical circuit contains many different devices and interconnects, making the parasitic effects more difficult to model as more and more structures are added to the chip. In order to keep the inductor as isolated as possible, patterned ground shields (PGS) and guard rings are used to capture the field lines before they reach other parts of the circuit.

PGS structures eliminate part of the substrate losses by terminating the inductor electric field before it reaches the lossy silicon substrate [20]. Guard rings are useful to prevent unwanted coupling with other parts of the circuit, but they have negative effect on the quality factor Q and reduce the SRF [21]. A good inductor modeling tool should be able to incorporate PGS structures an aid in the tradeoff problem of using guard rings. The substrate-loss canceling effect of a PGS could also help in the accuracy of a GP model by partially eliminating the substrate capacitance and resistance [3].

7 Conclusions

A geometric programming tool for inductor sizing was demonstrated. Equations were derived for each of the equivalent lumped circuit parameters and then adapted to become compatible with the posynomial form of geometric programs. The difficulty of modeling inductors over lossy substrate forces broad approximations that degrade the quality of the result. Nevertheless, good agreement is found for inductance and self resonance frequency, with the latter being influenced by the former. The solver runs in less than a second for each coil, which allows multiple geometries to be devised without the need for EM simulations. The presented model is easily extensible and can be enhanced by more accurate expressions and different optimization techniques that don't require fitting to posynomial forms.

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A Online Resources

The code used to produce the results in this paper is publicly available at [8].

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