Observations and Future Directions on Crystal-Free Clock and Data Recovery for Bluetooth Low-Energy

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Abstract

Recent developments in crystal-free Systems-on-Chips (SoCs) have shown promise in enabling communications on various wireless protocols. SCμM-3C [4] has been shown as a standards-compatible IEEE 802.15.4 node, with a demonstrated receiver sensitivity of −83 dBm. It has also been demonstrated as a Bluetooth Low-Energy (BLE) beacon [6], and most recently, its analog front-end has been demonstrated with a new FPGA-based digital baseband implementation as a BLE receiver achieving −82 dBm sensitivity, exceeding the −70 dBm requirement of the Bluetooth 4.0 specification. During BLE receiver experiments, however, systematic errors were observed with the clock and data recovery (CDR) schemes used in SCμM. Correction of these systematic errors should enable crystal-free platforms like SCμM to be widely usable as BLE nodes, more closely approaching the performance of traditional systems.

CCS Concepts

• **Hardware → Wireless devices**; **Sensor devices and platforms**; **Radio frequency and wireless circuits**; *System on a chip*; **Signal integrity and noise analysis**.

Keywords

Crystal-Free, Bluetooth Low Energy, IEEE 802.15.4, Clock and Data Recovery

1 Introduction

As shown in Table 1, the IEEE 802.15.4 2.4 GHz and Bluetooth LE 1M PHYs are extremely similar. It is reasonable to postulate that any capable 802.15.4 transceiver should be capable as a BLE 1M transceiver as well. This has directed research in previous years to develop the necessary hardware for BLE demodulation in an FPGA to interface with SCμM's analog front end [3]. While these efforts demonstrated similar receiver sensitivity for BLE 1M as has been shown in 802.15.4 (-82 dBm and -83 dBm, respectively), we believe that systematic errors limit the performance of SCμM in both of these scenarios. This paper serves to detail these observations and direct future developments towards improving performance on crystal-free BLE systems.

PHY	IEEE 802.15.4 2.4 GHz	Bluetooth LE 1M
Band	2.405 GHz to 2.480 GHz	2.402 GHz to 2.480 GHz
Channel Spacing	5 MHz	2 MHz
Bandwidth (peak)	250 Kbps	1 Mbps
Modulation Type	Half-Sine Shaping Offset-Quadrature Phase Shift Keying (HSS O-QPSK) [1]	Gaussian Frequency Shift Keying (GFSK)
Tone Spacing (Nominal)	1 MHz (± 500 kHz)	500 kHz (± 250 kHz)
Symbol/Chip Rate	2 MChips/s	1 MSymbols/s
Bits per Symbol/Chip	0.125 bits per Chip (4 bits = 32 chips)	1 bit per Symbol
Timing Indicator	40-bit Sync. Header (160 μs)	8-bit Preamble (8 μs)
Maximum RX Error Rate	6.5% Chip Error (1% Packet Error)	0.1% Bit Error (30.8% Packet Error)

[1] HSS O-QPSK is equiv. to Minimum Shift Keying (MSK) [5]

Table 1: Comparison of IEEE 802.15.4 2.4 GHz PHY and BLE 1M PHY. SCμM has been demonstrated previously as a fully capable 802.15.4 transceiver.

2 Observations

2.1 Matched Filtering

Matched Filtering is used for data recovery on SCμM, the output of which forms a clock signal used to sample the recovered data. As shown in [2], a well-designed matched filter implementation is suitable for Low-IF demodulation schemes, which are commonly used in crystal-free systems to avoid the penalty of higher flicker noise. While SCμM's implementation fits the guidelines in [2], its 4-bit analog-to-digital converters (ADCs) are at the low end of the recommendations. However, the data demodulation performance of the matched filter implementation is generally acceptable.

2.2 Clock Recovery

The clock recovery implementation is the predominant limitation in SCμM's performance as a BLE receiver. The clock recovery algorithm used on SCμM for IEEE 802.15.4 demodulation is based on [1]. This uses the digitized IF samples to calculate a complex-valued s-curve and uses the real component of this as the timing error estimate. We suspect that SCμM's 4-bit ADCs hurt the performance of this algorithm. When used for BLE clock recovery, extenuating issues further degrade performance. There are three main observations of this algorithm's performance that make it less suitable for BLE demodulation than IEEE 802.15.4 demodulation:

(1) S-curve magnitude is reduced by a frequency offset Δf

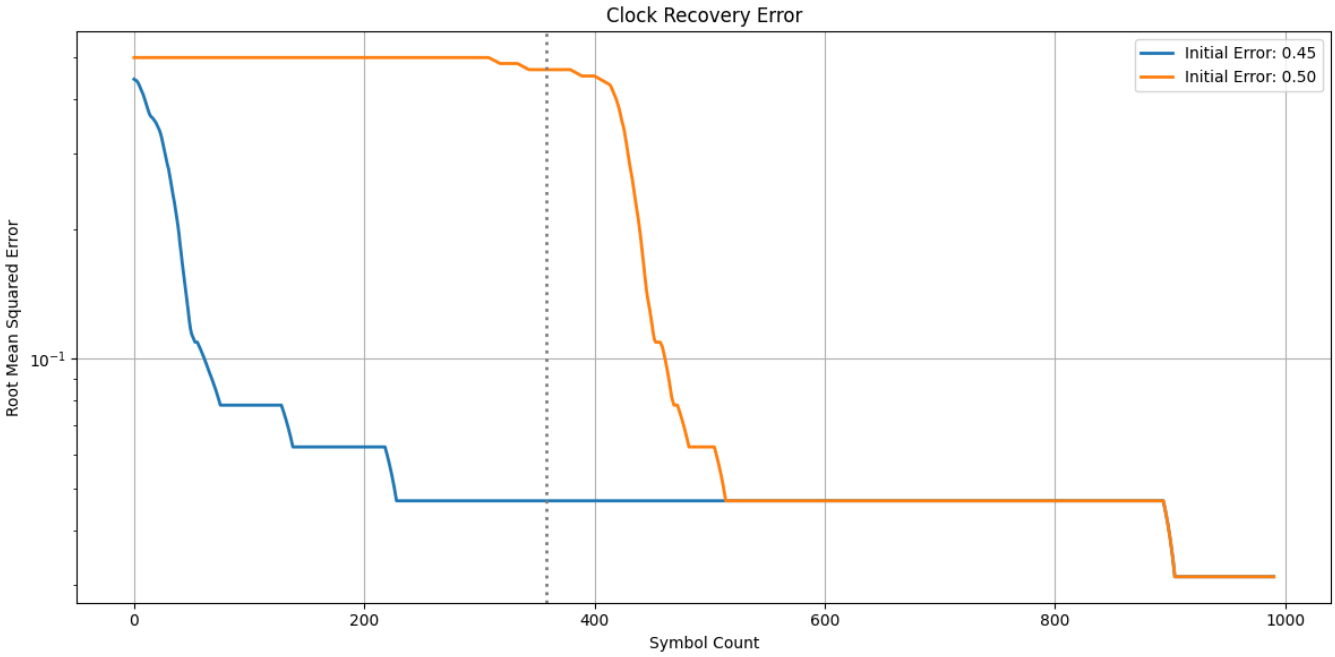

Figure 1: Clock Recovery acquisition time for 0.45T and 0.5T symbol error (T is symbol period). Simulation uses 12-bit ADCs at 64 samples/symbol. Acquisition time increases for both lower ADC bit depth and samples/symbol. Vertical dotted line represents the maximum-length BLE advertising packet

(2) Gaussian filtering reduces the s-curve magnitude, limiting the maximum calculated error
(3) Timing convergence for large initial errors is on the order of hundreds of symbols

SCμM's clock recovery implementation corrects for the frequency offset by applying a 180° rotation to the complex-valued s-curve. This correction factor is dependent on Δf, requiring a different correction factor for the different IF used in a BLE implementation. However, this correction factor assumes a constant frequency offset. This assumption does not hold in crystal-free systems, and as such a reduction in s-curve magnitude will always be present. Any reductions in s-curve magnitude increase the convergence time. This convergence time is the primary driver of systematic errors observed in BLE demodulation. A simulation of this implementation's convergence time is shown in Figure 1. The convergence time increases both with lower bit depth and sampling rate. As such, it is clear that, especially when starting with significant timing error (a common situation in crystal-free transceivers), timing is far from converged within a BLE packet duration, whereas it converges successfully in 802.15.4 packets. Reducing this convergence time appears to be critical to improve the performance of crystal-free BLE receivers.

3 Future Directions

While a complete overhaul isn't necessarily required, we suspect there are a few viable directions to investigate in order to improve the timing convergence of clock recovery algorithms used in crystal-free BLE demodulation. The first would be to use the known preamble (and possible access address) of BLE packets to determine an initial lock for the existing scheme. Another option would be to develop a transition-based timing detector (e.g., UART clock recovery), which would use the good matched filter output to detect timing based on its transitions. Such a scheme may also benefit from preamble detection. We believe advancements in this area will improve both crystal-free BLE and IEEE 802.15.4 receiver performance, possibly approaching that of state-of-the-art receivers.

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