A 32-channel event-based bio-signal analog front-end with adaptive delta and pulse frequency encoding

Shyam Narayanan, Saptarshi Ghosh, and Giacomo Indiveri
Institute of Neuroinformatics, University of Zurich and ETH Zurich
Zurich, Switzerland

Abstract

Low-power event-based Analog Front-Ends (AFEs) are essential for building efficient, end-to-end neuromorphic signal processing systems. In this paper, we present an event-based AFE Application-Specific Integrated Circuit (ASIC) optimized for biomedical signal acquisition and encoding. The chip features 32 independently programmable input channels with dual-mode encoding mechanism outputs, comprising Pulse Frequency Modulation (PFM) and adaptive Asynchronous Delta Modulator (aADM) circuits. The aADM encoder provides an auto-scaling mechanism that adapts the encoding data rate based on the input signal envelope in real time, enabling very high data compression for low-power information transmission. This approach paves the way toward adaptive wireless communication of neural signals for on-line processing in brain-computer interfaces. Fabricated in a 180 nm CMOS process, the proposed ASIC offers a highly configurable interface compatible with state-of-the-art Spiking Neural Network (SNN) neuromorphic processors.

Keywords

Neuromorphic, Analog Front-End, Spiking Neural Network, Delta Modulation, Adaptive Threshold, Brain-Computer Interfaces

1 Introduction

Spiking Neural Network (SNN) implemented on bio-inspired neuromorphic hardware provide a low-power, event-driven signal processing paradigm, ideally suited for handling streaming data on the edge [6, 12, 20]. To leverage SNN-based data processing pipelines effectively, highly efficient event-based front-ends are required to convert analog sensory signals into the appropriate Address-Event Representation (AER) [10].

Several bio-signal processing systems have already been proposed in the past that included dedicated asynchronous circuits for low-power and low-latency event-based encoding [5, 14, 15, 18, 23, 27]. However, typically those encoding circuits use fixed reference threshold levels for data conversion. This strategy faces severe limitations when scaling the converters to large multi-channels or operating them long-term in real world Brain Computer Interface (BCI) scenarios [1, 28]: fixing the thresholds too closely will generate large amounts of events for noisy signals; conversely, placing the thresholds too far apart to avoid encoding noise fluctuations will also reduce the encoding accuracy of the signal, degrading the downstream feature extraction. To overcome these limitations, we present the first realization of an adaptive Asynchronous Delta Modulator (aADM) that can autonomously adapt the reference threshold levels to the noise levels present in the input signal, building on the circuit originally proposed in [26]. Such combined ADM and Pulse Frequency Modulation (PFM) encoding has previously been demonstrated in a 16-channel event based AFE with a fixed delta-threshold (SPAIC [23]); the present work's contribution is the integration and full on-silicon characterization of an adaptive threshold-generation circuit within a scaled, 32-channel ASIC. Specifically, we designed and fabricated *PHOENIX* (Pre-processing Hardware for Optimally Encoding Neuromorphic processor's Input X-modal signals), a 32-channel Application-Specific Integrated Circuit (ASIC) with configurable and adaptive sensory signal conditioning for efficient event encoding. The Analog Front-End (AFE) circuits are explicitly optimized to operate at the low end of the frequency spectrum to process physiological signals. The novel implementation of the aADM circuit dynamically adjusts the reference threshold in real-time, by following the envelope of the input signal. This allows it to encode only the meaningful parts of the signal, and to reject the noise floor present in the signal. By configuring the amount of adaptation, this circuit can adjust the data encoding and compression ratio at the sensor level, providing a trade-off between desired raw signal reconstruction accuracy and on-line information processing needs (e.g., to just detect the occurrence of a real action potential, or to classify specific spatio-temporal patterns). This approach makes this ASIC suitable for both scaling up to massive multi-channel bio-signal processing and encoding arrays, and for transmitting multi-channel asynchronous AER events with low-bandwidth and low-latency.

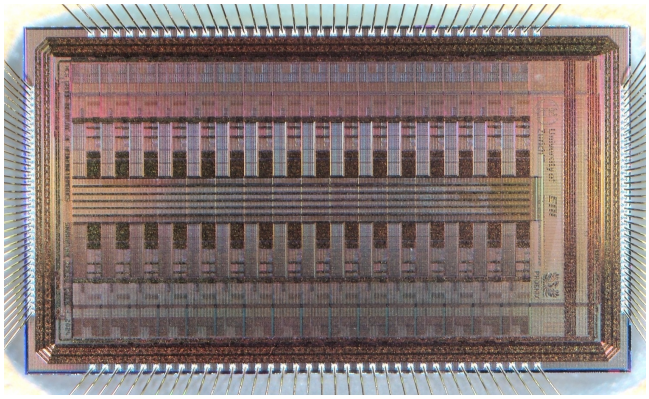

Figure 1: AFE chip micrograph, with 32 mixed-signal analog/digital processing blocks, a synchronous digital Serial Peripheral Interface (SPI) input interface, and an asynchronous AER output interface.

2 ASIC architecture

The chip comprises 32 analog processing channels that pre-condition the signal with amplification, filtering stages, and event-encoding circuits that convert the input signal into asynchronous discrete events, using parallel encoding methods: pulse-frequency modulation, via a low-power Leaky Integrate and Fire (LIF) neuron, and adaptive delta-modulation, via an aADM circuit. The analog circuit parameters can be programmed using an on-chip temperature compensated bias generator [8, 9]. All chip configurations, including the bias-generator, an 8 bit Capacitor DAC (CDAC) for filter parameters, and a 7 bit Voltage DAC (VDAC) for aADM block controls, are programmed via a digital SPI based interface. The asynchronous output events generated by each channel are channeled through an arbiter tree and transmitted off-chip using the AER communication protocol [3, 7]. The ASIC measures 3.22 mm × 5.67 mm and is fabricated in the standard XFAB 180 nm process. A micrograph of the fabricated chip is shown in Fig. 1.

An illustration of the ASIC building blocks and its signal processing pipeline is presented in Fig. 2. The processing chain for each input channel consists of four main stages: a Low-Noise Amplifier (LNA), a fourth-order Band-Pass Filter (BPF), a Programmable Gain Amplifier (PGA), and the dual-mode event-based encoding block (aADM and PFM).

2.1 Pre-encoding circuit implementation

2.1.1 Low noise gain stages (LNA and PGA): For modularity, both the LNA and PGA rely on the same Operational Transconductance Amplifier (OTA) core, which is based on a wide input range current-mirror-type architecture to accommodate large input variations [11]. The amplifiers are operated in a closed loop as capacitive feedback amplifiers utilizing a DC-Servo loop implemented with pseudo-resistors [19, 23] (see Fig. 2) . The LNA amplifies weak input signals with a tunable gain ranging from 0 dB to 22 dB, controlled by a 4 bit binary weighted CDAC.

2.1.2 The Band-Pass Filter (BPF). Every AFE channel has a 4th-order BPF with tunable center frequency ω_0 and quality factor (Q). The filter is based on a Flipped Voltage Follower (FVF) topology (see Fig. 2) to achieve better noise performance due to the inherent current reuse present in the architecture [16]. The filter's center frequency ω_0 is tunable with the on-chip bias generator [9]. The capacitors of this filter are implemented as an 8 bit CDAC. By configuring C_1 and C_2 (see Fig. 2), the (Q) and center frequency (ω_0) can be configured in a precise way with a resolution of $C_{1,2}/2^8$ steps, as described in Eq. (1).

$$\omega_0 = \sqrt{\frac{gm_1 \cdot gm_2}{C_1 \cdot C_2}}, Q = \sqrt{\frac{gm_2 \cdot C_2}{gm_1 \cdot C_1}} \tag{1}$$

Where gm_1 and gm_2 are the transconductances of transistors P_1 and P_2 of FVF filter shown in Fig.2 As each filter's center frequency (ω_0) and quality factor (Q) are programmable, they can be configured as a parallel filter banks or as identical parallel electrode interface channels. The PGA following the BPF adds additional gain to the signal. The combined frequency response of the BPF & PGA chain can be tuned by adjusting the bias current of the filter and the gain adjustment of the PGA, providing the necessary amplification at requisite frequency range, depending on the application, the signal and noise level for optimal encoding.

2.2 Adaptive Asynchronous Delta Modulator encoding

The basic Asynchronous Delta Modulator (ADM) circuit [5] belongs to a class of level crossing Analog-to-Digital Converters (ADCs) where the sampling interval is adapted based on the characteristics of the coded signal [13]. In its classic form it comprises two comparators with a fixed reference threshold (termed as *delta threshold*) acting as a level shifter around a base line. This setup outputs an event based on the difference in the amplitude of a signal, when the change is compared with two known thresholds (termed as up- and down- delta thresholds) set by an on-chip VDAC to encode both upward and downward swings of the input. An *'UP'* or *'DN'* tag is attached to the output event based on the polarity of the change, *i.e.*, if the signal has increased (upward swing) or decreased (downward swing) at the level crossing more than the set reference threshold. The on-chip AER interface produces a *'REQ'* signal to transmit the address of the sending node off-chip (see Fig. 2). Once acknowledged off-chip, the chip-level acknowledge signal *'ACK'* is converted back into a per-channel signal (*'CH_ACK'*). This signal is gated with a current-controlled (I_{RFR}) inversion stage to create a *'RESET'* mechanism with a refractory period in each channel that resets the aADM circuit.

This approach asynchronously digitizes and encodes relevant changes in the input signal, based on the set delta threshold. The accuracy of conversion therefore depends on the chosen fixed delta-threshold. Low thresholds will produce a high data rate, allowing even lossless reconstruction, while higher thresholds will lead to lower data rates, at the cost of lower reconstruction accuracy. In real-world applications, such as long-term multi-channel monitoring in biomedical or BCI domains, input signals are naturally affected by noise, and the noise profile can change and drift with time. In these cases, a fixed delta threshold might become non-ideal. The solution implemented here is based on an adaptive scheme that changes the delta threshold based on the frequency changes of the input signal envelope, but still encoding its high amplitude-high frequency fluctuations [26]. The schematic diagram of the circuit we designed and fabricated in the ASIC including additional blocks (fixed gain stage, 7 bit Digital-to-Analog Converter (DAC), Adaptive Threshold Generation) is presented in Fig. 3.

2.2.1 Adaptive Delta threshold generation. The adaptive delta threshold generation block consists of four stages. The input signal from the preceding signal conditioning stage (with gain and filtering circuits) flows into the adaptive delta generator circuit (Fig. 3, highlighted in grey) with a fixed gain of $A = 4$. Figure 4 presents the four stages of the delta generator. The first stage is an envelope extractor which is implemented using a subthreshold Source Follower (SF) circuit (Fig. 4, left). This extracted envelope is then fed into two Differential Pair Integrator (DPI) circuits, which act as current-mode low-pass filters, when operated in the subthreshold regime [2, 4].

The outputs of the two DPIs are then compared with a current mode Winner-Take-All (WTA) circuit [17] to detect a rapid change in signal and to adapt the threshold of the ADM. In the current

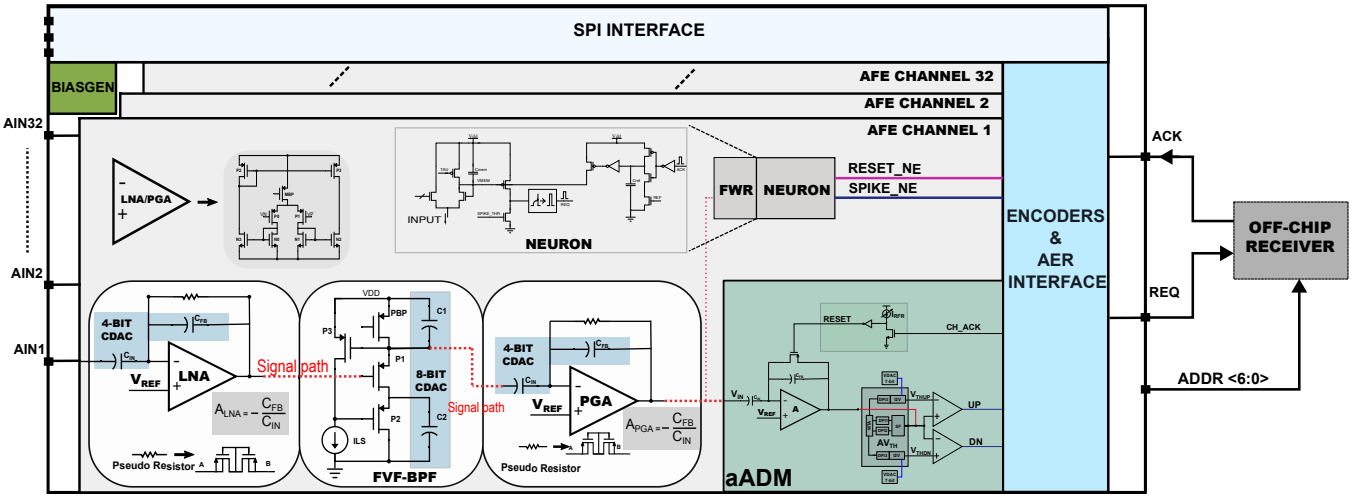

Figure 2: Chip block diagram detailing one of the 32 analog channels connected to the shared BiasGen, SPI, and AER interface blocks.

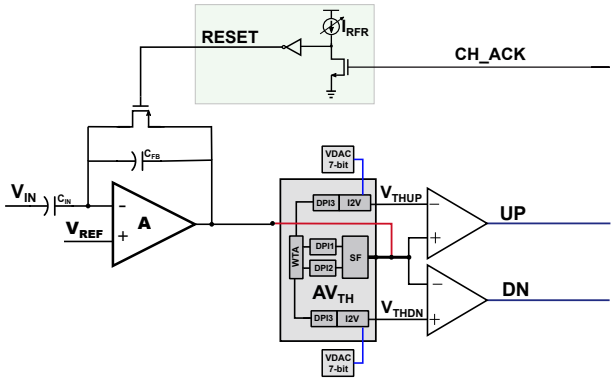

Figure 3: Circuit-level schematic of the aADM circuit with two comparators and thresholds being generated by the adaptive block, highlighted in grey.

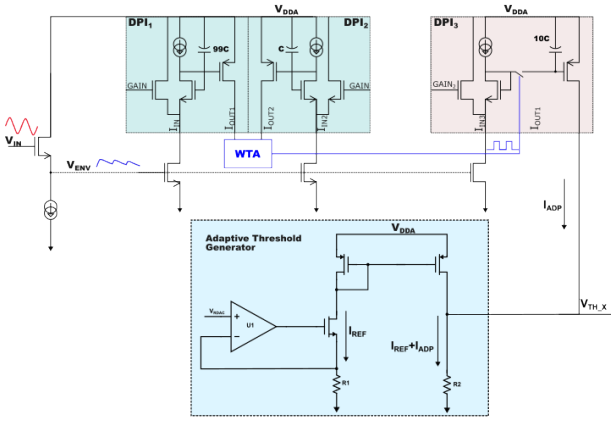

Figure 4: Circuit-level schematic of the adaptive delta threshold generator with a source-follower envelope extractor, three DPIs and one WTA block supplying the delta threshold to the comparators of the aADM circuit.

silicon implementation, the capacitor used in DPI_1 is 99 times that of DPI_2 to produce a large difference in time constants between the two filters, so that the circuit can determine fast changing signals. The WTA picks the winner and triggers a sampling operation in DPI_3 [26]. The output current of DPI_3 therefore is proportional to the very low-frequency components of the input signal envelope, and neglects the fast transients (such as action potentials) present in the signal. This current is then added to or subtracted from the baseline threshold, encoded as current and generated by a current to voltage converter (marked as Adaptive Threshold Generator in Fig. 4). The composite current is then converted back to voltage within the same block, generating the final adaptive delta threshold voltage (VTH_X). For the 'UP' threshold the adaptive current is added to the baseline, and for 'DN' one it is subtracted from the baseline.

2.3 Pulse frequency modulation

The PFM encoder is realized using an Adaptive Exponential Integrate-and-Fire (AdExp-IF) circuit [24] using previously proposed topology schemes [23]. This result is obtained by first converting the amplified and filtered voltage into a current, and then by sending it directly as input to the AdExp-IF silicon neuron. The voltage-to-current conversion is carried out by a wide-range transconductance amplifier with source degeneration to extend the linearity. The current is then full-wave rectified and subsequently copied to the neuron input (see Fig. 2). As PFM encoding of signals has been amply described in the literature and demonstrated across many implementations [23], in this work we focus mainly on the aADM results. However, preliminary measurements on this chip proved this section to be functional as well.

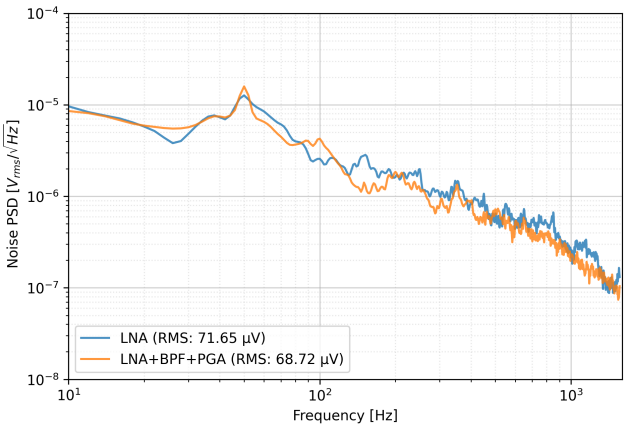

Figure 5: Input Referred Noise Power Spectral Density integrated from 10 Hz to 1.6 kHz.

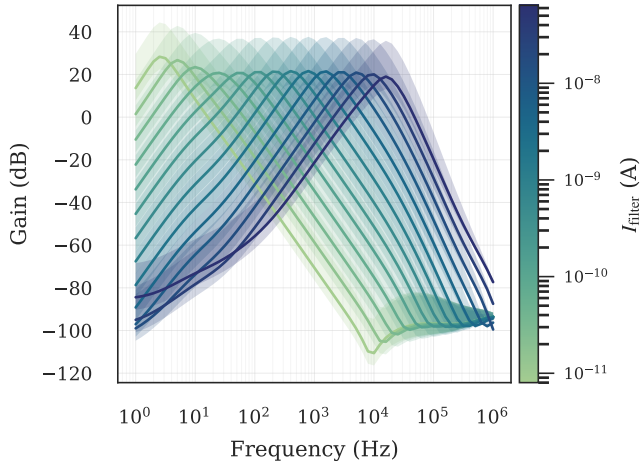

Figure 6: Frequency Response of LNA-BPF-PGA Chain and Gain Configurations. The solid lines are the mid-gain code=7, shaded area depicts the 0-15 gain-code range

3 Measurement results

The initial silicon measurements reported in this section verify the chip's functionality.

3.1 Noise measurement

Noise analysis of a typical analog front end can be modeled as:

$$v^2_{n,AFE} = v^2_{n,LNA} + \frac{v^2_{n,BPF}}{A^2_{LNA}} + \frac{v^2_{n,PGA}}{A^2_{LNA}A^2_{BPF}} + \frac{v^2_{n,ENCODER}}{A^2_{LNA}A^2_{BPF}A^2_{PGA}} \quad (2)$$

The overall input referred noise of the chain is dominated by the first stage in the chain, namely the LNA and its gain. The gain of the following stages helps in reducing the fractional term in Eq. 2. The LNA circuit could be further optimized to reduce its noise levels, however at the cost of larger area allocation.

The initial silicon characterization of the AFE signal chain was performed to quantify the programmable gain control and noise performance. The measurement results of the gain and frequency response of the chain is shown in Figs. 6 and 5. The measurement of the LNA-BPF-PGA chain over a target biomedical bandwidth of 1.6 kHz demonstrated an input-referred noise power spectral density integrating to 68.72 μV_{rms} (see figs. 6 & 5).

3.2 Encoding

A circuit-level simulation showing the internal signals of the adaptive delta threshold circuit is shown in Fig. 7a. Both an input signal (pure-tone sinusoid), amplitude modulated with a staircase function and added white noise, representing changing noise floors in a realistic control-input are shown. The input was first amplified through the gain stages before being fed into the adaptive generator block. The input to the adaptive generator block as well as the output delta ('UP' and 'DN') thresholds (depicted in blue and green lines) are depicted in relation to the input in Fig. 7a. The encoded events are presented as logic pulses showing the fast adaptation with changing noise floors in the staircase signal. Figure 7b demonstrates that after adaptation, the addition of an event of interest (e.g., an action potential in a neural recording) will encode it reliably with additional events, despite having adapted to the high noise floor.

Figure 8 shows experimental measurements of an analogous experiment run directly on the ASIC. The synthetic control stimulus was scaled appropriately to 20 mV amplitude and played into the chip. In order to match the silicon measurement with simulation, just one channel was enabled with the rest of the channels disabled. The voltage shown in Fig. 8 is a real oscilloscope capture of the PGA output signal. The events of the aADM were recorded at the output in the form of the AER with external handshaking hardware in the loop. The chip recorded data demonstrates adaptation in the recorded events while encoding the event of interest near $t = 1.7$ s, validating the hardware implementation of the adaptive event-encoding circuit.

4 Conclusions

We successfully demonstrated the operation of an adaptive event-based analog front-end ASIC with 32 parallel channels, featuring extensive programmability via SPI, and supporting the AER output protocol commonly used by neuromorphic SNN processors. By implementing the aADM encoder alongside a standard PFM encoder, the proposed ASIC resolves the critical issue of automated reference threshold generation in multi-channel or long-term biomedical sensing [25] while providing sensor-level tunable data encoding. A typical chronic, multi-channel BCI recording from wearable multi-electrode array spans tens to hundreds of channels [21, 28], where each channel must digitize local field potentials and/or neural action potentials within the sub-2 kHz band for hours to days. In such cases, the noise floor can drift independently across channels due to electrode-tissue impedance changes, motion artifacts, and channel-to-channel variability. As the aggregate event rate across all channels is constrained by the wireless telemetry link's power and bandwidth budget, a fixed delta-threshold, chosen *a priory*, can either saturate the AER output during artifact-heavy periods on

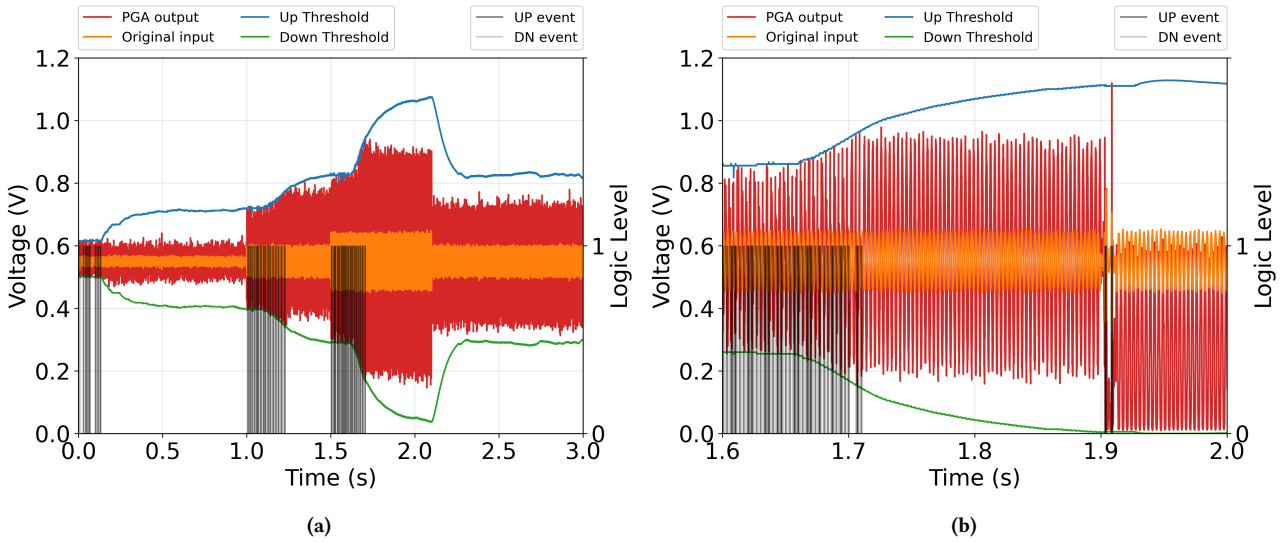

Figure 7: Circuit-level simulation of the aADM block showing changing threshold based on the input signal; (a) shows a noisy input signal with staircase amplitude, changing threshold, and corresponding encoded events. (b) Zoomed-in part of the simulation, with an additional pulse artificially added to the input signal, to represent an action potential or event of interest at t=1.9s. As expected, the encoder responds to this high-frequency input pulse even after the aADM has adapted to the highest noise levels.

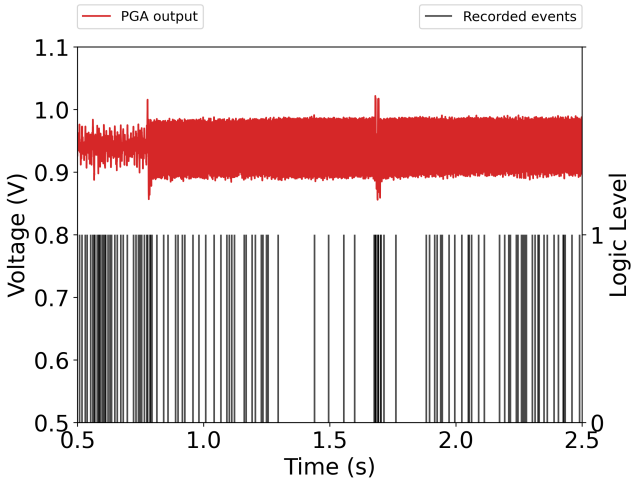

Figure 8: Chip measurements showing aADM events in response to the control stimulus with step in the noise level at t = 0.6 s approximately, and with an input event of interest at approximately t = 1.7 s. Note that 'UP' and 'DN' events are merged in the current measurement setup.

noisy channels, or miss low-amplitude transients of interest on quieter ones once thresholds are raised uniformly to suppress noise. The proposed aADM's per-channel, real time reference threshold adaptation resolves this trade-off directly, allowing each channel to adapt independently to its own noise envelope while still capturing fast, high-amplitude events of interest and reducing the data volume that must be transmitted off-chip. This architectural solution positions the *PHOENIX* ASIC as a versatile companion front-end for interfacing such signals directly with asynchronous SNN processors. Future work will target extending this validation to chronic in-vivo multi-channel recordings, quantifying the data transmission efficiency impact on downstream decoding and on the system-level power and bandwidth budget when interfaced with an SNN back-end such as DYNAP-SE [22], alongside integration into a fully wireless, multi-channel head stages for next-generation biomedical sensing applications.

Acknowledgments

We would like to thank Chenxi Wen the Institute of Neuroinformatics, University of Zurich and ETH Zurich for carrying out the circuit-level simulations of the aADM used in Fig. 7, Tugba Demici for feedback and fruitful discussions on the AER circuits, Zhe Su and Arianna Rubino for support in the design of the asynchronous digital circuits and silicon neurons respectively.

Part of this work was supported by the Swiss National Science Foundation (SNSF projects 204651 and 217160). During the preparation of this work, the author(s) used generative AI tools to assist with language editing and revising the manuscript text, including improving sentence structure, clarity, and adherence to academic style conventions. The tool(s) was used solely to improve clarity, grammar, and readability of author-written content. The tool(s) was not used to generate original scientific content, data, analysis, or conclusions. After using this tool, the author(s) reviewed and edited the content as necessary and take(s) full responsibility for the accuracy and integrity of the final content of the article.

References

[1] Jim Bartels, Olympia Gallou, Hiroyuki Ito, Matthew Cook, Johannes Sarnthein, Giacomo Indiveri, and Saptarshi Ghosh. 2025. Event driven neural network on a mixed signal neuromorphic processor for EEG based epileptic seizure detection. *Scientific Reports* 15, 1 (May 2025). doi:10.1038/s41598-025-99272-6

[2] C. Bartolozzi, S. Mitra, and G. Indiveri. 2006. An ultra low power current–mode filter for neuromorphic systems and biomedical signal processing. In *Biomedical Circuits and Systems Conference, (BioCAS)*. IEEE, 130–133. doi:10.1109/BIOCAS.2006.4600325

[3] K.A. Boahen. 2000. Point-to-Point Connectivity Between Neuromorphic Chips Using Address-Events. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 47, 5 (2000), 416–34. doi:10.1109/82.842110

[4] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri. 2014. Neuromorphic electronic circuits for building autonomous cognitive systems. *Proc. IEEE* 102, 9 (Sept. 2014), 1367–1388. doi:10.1109/JPROC.2014.2313954

[5] F. Corradi and G. Indiveri. 2015. A Neuromorphic Event-based Neural Recording System for Smart Brain-Machine-Interfaces. *Biomedical Circuits and Systems, IEEE Transactions on* 9, 5 (2015), 699–709. doi:10.1109/TBCAS.2015.2479256

[6] Federico Corradi, Amir Zjajo, Letícia Maria Bolzani Poehls, Miloš Krstić, Orlando Moreira, Zeqi Zhu, and Farhad Merchant. 2025. Neuromorphic Edge Computing: Challenges, Opportunities, and Current Solutions. In *2025 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*. IEEE, 1–7. doi:10.1109/islped65674.2025.11261768

[7] S. Deiss, R. Douglas, M. Fischer, M. Mahowald, and T. Matthews. 1994. *Multiplexor bus and local address event bus protocol.* Technical Report. Applied Neurodynamics, MRC Anatomical Neuropharmacology Unit, Research Machines.

[8] T. Delbruck, R. Berner, P. Lichtsteiner, and C. Dualibe. 2010. 32-bit Configurable bias current generator with sub-off-current capability. In *International Symposium on Circuits and Systems, (ISCAS)*. IEEE, IEEE, Paris, France, 1647–1650. doi:10.1109/ISCAS.2010.5537475

[9] T. Delbruck and A. Van Schaik. 2005. Bias Current Generators with Wide Dynamic Range. *Analog Integrated Circuits and Signal Processing* 43, 3 (2005), 247–268.

[10] Wenzhe Guo, Mohammed E Fouda, Ahmed M Eltawil, and Khaled Nabil Salama. 2021. Neural coding in spiking neural networks: A comparative study for robust neuromorphic systems. *Frontiers in Neuroscience* 15 (2021), 638474.

[11] R.R. Harrison and C. Charles. 2003. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE Journal of Solid-State Circuits* 38, 6 (June 2003), 958–965. doi:10.1109/JSSC.2003.811979

[12] Giacomo Indiveri. 2025. Neuromorphic is dead. Long live neuromorphic. *Neuron* (Oct. 2025), 1–4. doi:10.1016/j.neuron.2025.09.020

[13] HIROSHI Inose, T Aoki, and K Watanabe. 1966. Asynchronous delta-modulation system. *Electronics Letters* 3, 2 (1966), 95–96.

[14] M. Judy, A.M. Sodagarand, R. Lotfi, and M. Sawan. 2014. Nonlinear signal-specific ADC for efficient neural recording in brain-machine interfaces. *IEEE transactions on Biomedical Circuits and Systems* 8, 3 (2014), 371–381.

[15] Ye Ke, Zhengnan Fu, Junyi Yang, Hongyang Shang, and Arindam Basu. 2026. A 1024-Channel 0.8V 23.9-nW/Channel Event-Based Compute In-Memory Neural Spike Detector. *IEEE Transactions on Biomedical Circuits and Systems* 20, 3 (2026), 342–354. doi:10.1109/TBCAS.2025.3642865

[16] Kwantae Kim and Shih-Chii Liu. 2023. Continuous-Time Analog Filters for Audio Edge Intelligence: Review on Circuit Designs. *IEEE Circuits and Systems Magazine* 23, 2 (2023), 29–48. doi:10.1109/mcas.2023.3267893

[17] J. Lazzaro, S. Ryckebusch, M.A. Mahowald, and C.A. Mead. 1989. Winner-take-all networks of $O(n)$ complexity. In *Advances in neural information processing systems (NIPS)*, D.S. Touretzky (Ed.), Vol. 2. Morgan Kaufmann, San Mateo - CA, 703–711.

[18] Yongjia Li, Duan Zhao, and Wouter A. Serdijn. 2013. A Sub-Microwatt Asynchronous Level-Crossing ADC for Biomedical Applications. *IEEE Transactions on Biomedical Circuits and Systems* 7, 2 (April 2013), 149–157. doi:10.1109/tbcas.2013.2254484

[19] Can Livanelioglu, Woojun Choi, Donghwan Kim, Jiawei Liao, Rosario Incandela, Giorgio Cristiano, and Taekwang Jang. 2022. A 0.0014 mm², 1.18 TΩ Segmented Duty-Cycled Resistor Replacing Pseudo-Resistor for Neural Recording Interface Circuits. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 62–63. doi:10.1109/vlsitechnologyandcir46769.2022.9830140

[20] Vivek Mohan, Wee Peng Tay, and Arindam Basu. 2025. Towards neuromorphic compression based neural sensing for next-generation wireless implantable brain machine interface. *Neuromorphic Computing and Engineering* 5, 1 (Jan. 2025), 014004. doi:10.1088/2634-4386/adad10

[21] Vivek Mohan, Wee Peng Tay, and Arindam Basu. 2025. Towards neuromorphic compression based neural sensing for next-generation wireless implantable brain machine interface. *Neuromorphic Computing and Engineering* 5, 1 (2025), 014004.

[22] S. Moradi, N. Qiao, F. Stefanini, and G. Indiveri. 2018. A Scalable Multicore Architecture With Heterogeneous Memory Structures for Dynamic Neuromorphic Asynchronous Processors (DYNAPs). *IEEE Transactions on Biomedical Circuits and Systems* 12, 1 (Feb. 2018), 106–122. doi:10.1109/TBCAS.2017.2759700

[23] Shyam Narayanan, Matteo Cartiglia, Arianna Rubino, Charles Lego, Charlotte Frenkel, and Giacomo Indiveri. 2023. SPAIC: A sub-μW/Channel, 16-Channel General-Purpose Event-Based Analog Front-End with Dual-Mode Encoders. In *Biomedical Circuits and Systems Conference (BioCAS)*. IEEE. doi:10.1109/biocas58349.2023.10388815

[24] Arianna Rubino, Can Livanelioglu, Ning Qiao, Melika Payvand, and Giacomo Indiveri. 2020. Ultra-Low-Power FDSOI Neural Circuits for Extreme-Edge Neuromorphic Intelligence. *IEEE Transactions on Circuits and Systems I: Regular Papers* 68, 1 (2020), 45–56. doi:10.1109/TCSI.2020.3035575

[25] Mohammadali Sharifshazileh, Karla Burelo, Johannes Sarnthein, and Giacomo Indiveri. 2021. An electronic neuromorphic system for real-time detection of High Frequency Oscillations (HFOs) in intracranial EEG. *Nature Communications* 12, 1 (2021), 1–14. doi:10.1038/s41467-021-23342-2

[26] Mohammadali Sharifshazileh and Giacomo Indiveri. 2023. An Adaptive Event-based Data Converter for Always-on Biomedical Applications at the Edge. *International Symposium on Circuits and Systems, (ISCAS)* (May 2023). doi:10.1109/iscas46773.2023.10181549

[27] Jonah Van Assche and Georges Gielen. 2020. Power Efficiency Comparison of Event-Driven and Fixed-Rate Signal Conversion and Compression for Biomedical Applications. *IEEE Transactions on Biomedical Circuits and Systems* 14, 4 (Aug. 2020), 746–756. doi:10.1109/tbcas.2020.3009027

[28] Tansel Baran Yasar, Peter Gombkoto, Alexei L. Vyssotski, Angeliki D. Vavladeli, Christopher M. Lewis, Bifeng Wu, Linus Meienberg, Valter Lundegardh, Fritjof Helmchen, Wolfger von der Behrens, and Mehmet Fatih Yanik. 2024. Months-long tracking of neuronal ensembles spanning multiple brain areas with Ultra-Flexible Tentacle Electrodes. *Nature Communications* 15, 1 (2024). doi:10.1038/s41467-024-49226-9